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Floating-Gate MOSFET Parallel Analog Network for Assignment Problems

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Abstract – **Floating-Gate-MOS Transistor (FGMOSFET) has several applications on analog circuit design; in some cases FGMOSFET simplifies high-complexity circuits because of its inherent properties. On the other side, working with FGMOSFET on subthreshold regime has allowed non-linear function implementation such as exponential and natural logarithm functions. Moreover, working on subthreshold regime is one of the most useful techniques for low-power designs.**

Taking advantage of FGMOSFET's properties, this work shows an analog CMOS circuit that finds the best solution of the combinatorial task of assignments in terms of Lagrange multipliers. This is in contrast to the Hopfield paradigm, which is often VLSI-costly. The building block in this circuit uses FGMOSFET transistors, has low silicon complexity and exhibits good electrical performance according to PSpice simulations. Final simulations were developed for a 0.5µm CMOS technology and the output currents reach an optimal solution in all cases. It might include threshold voltage programming circuits for reducing mismatch effects.

Key-words- **Assignment Problem, Floating Gate Transistor, subthreshold regime**

I. Introduction

That digital circuit design would replace analog circuit design was predicted a few years ago. However, the current technologies demand for faster, smaller and more complex circuits, at this point, analog design is useful in some applications.

Currently, analog design has many applications (being 20% of the current IC market), such as neuromorphic and communication circuits, that require greater processing velocities, less power consumption and smaller sizes, which many times is achieved through an analog solution. In the analog scenario, FGMOSFET has reached a place as a key element for certain designs and several works have been done about it. Specifically, FGMOSFET has allowed designing less complex circuits and programming analog circuits in order to avoid mismatch problems in MOS designs [1].

Besides, it has been used as a key element in memory blocks [2] and because of its analogy with biologic neuron, is a main component in some neural circuits [3]. Alternatively, FGMOSFET allows non-linear function implementations by working on subthreshold regime [4].

This advantage is used in this work to implement an analog network which solves the well-known Assignment Problem; the method by Urahama [5] that uses Lagrange multipliers is suitable for integration in silicon with present FGMOSFET as an analog parallel circuit.

II. Floating Gate Transistor Working On Subthreshold Regime

FGMOSFET is a multiple-input device whose gate is surrounded completely by a dielectric material. A potential in the floating gate is induced by applying voltage at its inputs.

The floating gate voltage [6] is given by the Eq. 1

$$V_{FG} = \sum_i \frac{C_i}{C_{TOT}} V_i + \frac{C_{GS}}{C_{TOT}} V_S + \frac{C_{GB}}{C_{tot}} V_B + \frac{C_{GD}}{C_{TOT}} V_D + \frac{Q_{FG}}{C_{TOT}} \quad (1)$$

Where C_i is the input capacitance, C_{GS}, C_{GB}, C_{GD} are gate-source, gate-bulk and gate-drain capacitances respectively and they are parasitic capacitances. Vi is the input voltage and V_S, V_B, V_D are the source, bulk and drain voltages respectively, Q_{FG} is the initial trapped charge in the floating gate during the fabrication process and it is an unknown quantity. Total capacitance, C_{TOT} is given by Eq. (2).

$$C_{TOT} = \sum_i C_i + C_{GS} + C_{GB} + C_{GD} \quad (2)$$

The relationship between the input capacitance and total capacitance is known as the capacitive coupling factor and this value is always less than one.

The FGMOSFET drain current working in subthreshold regime [6] is given by Eq. (3):

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$$I_D = I_0 \exp\left(\sum_{i=1}^{n} \frac{C_i}{C_{TOT}} \frac{V_{iS}}{nv_t} + \frac{C_{GD}}{C_{TOT}} \frac{V_{DS}}{nv_t} + \frac{Q_{FG}}{C_{TOT} nv_t}\right) \quad (3)$$

Where I_0 is the subthreshold current factor, v_t is the thermal voltage (26 mV approximately) and n is the swing factor. As Eq. 3 shows, drain current expression for a FGMOSFET working on subthreshold region includes an exponential term, which is used in this work to implement non-linear functions.

III. The Assignment Problem

The Assignment Problem falls into combinatorial optimization area, which can be explained by the job assignment paradigm, which consists on assign n jobs to n workers, where every assignment has a cost. The problem deals with finding the optimal assignment by minimizing the total cost [7]. The Assignment Problem can be expressed mathematically through Eqs. (4) , (5) and (6).

$$\text{Min} \quad \sum s_{ij} x_{ij} \quad \text{for i,j} = 1,2,\ldots,N \quad (4)$$

$$\text{Subject to} \sum x_{ij} = 1 \quad \text{for i} = 1,2,\ldots,N \quad (5)$$

$$\sum x_{ij} = 1 \quad \text{for j} = 1,2,\ldots,N \quad (6)$$

Where s_{ij} is the element ij of the cost matrix, Eqs. (5) and (6) represent the constraints of the system. Also, the discrete variables x_{ij} can take the values 0 or 1 and the solution is a permutation matrix X_{SOL}. In particular, searching this matrix for a large dimension is important in many real-time applications [8], which would demand mainly digital technology

IV. Solution Of The Assignment Problem Using Lagrange Multipliers

The work in [5] introduces electrical analog macromodels for solving a group of combinatorial optimization problems and that in [9] presents the mathematical proofs of finding their optimal solution by means of Lagrange multipliers.

The solution of the Assignment Problem consists on add a new term on equation (4) called "entropy". This new term allows the new objective function given by Eq. (7) to be a convex function which ensures a unique solution.

$$\min \sum_{i,j} s_{ij} x_{ij} + T \sum \sum x_{ij} \ln x_{ij} \quad (7)$$

Where Lagrangian function is given by Eq. (8). And the global minimum point is given when the gradient of (8) is equal to zero. So, the solution of equation system is given by Eqs. (9), (10) and (11).

$$L = \sum_{i=1}^{n}\sum_{j=1}^{n} s_{ij} x_{ij} + T\left[\sum_{i=1}^{n}\sum_{j=1}^{n} x_{ij} \ln x_{ij} + \sum_{i=1}^{n}\left(P_i - \frac{1}{2}\right)\left(\sum_{j=1}^{n} x_{ij} - 1\right) + \sum_{j=1}^{n}\left(Q_j - \frac{1}{2}\right)\left(\sum_{i=1}^{n} x_{ij} - 1\right)\right] \quad (8)$$

Where P_i and Q_j are the Lagrange multipliers. The number of Lagrange multipliers depends on the dimension of the cost matrix, which is a square matrix. For dimensions of n x n, the number of the multipliers is 2n.

$$x_{ij} = \exp -\left(\frac{s_{ij}}{T} + P_i + Q_j\right) \quad (9)$$

$$\frac{dP_i}{dt} = \sum_{j=1}^{n} x_{ij} - 1 \quad (10)$$

$$\frac{dQ_j}{dt} = \sum_{i=1}^{n} x_{ij} - 1 \quad (11)$$

Eqs. (10) and (11) represents a dynamic system, where T is the "temperature" term that selects the quality of the zero-one representation of the solution when the dynamic system has reached the steady state. When T is zero, the solutions will be distinguished of the non-solutions variables. However, in practice, T cannot be zero, so a enough small value is chosen.

V. Analog Design

The parallel Eqs. (9), (10) and (11) map into the current-mode array in Fig. 1 following the KCL, where 2n connection wires define the "Lagrange nodes" with voltages: $V_{P1}, \ldots, V_{Pn}, V_{Q1}, \ldots, V_{Qn}$. At the reference building block (i, j), the values V_{Sij} , V_{Pi} and V_{Qj} act as s_{ij}, P_i and Q_j in Eq. (9), respectively and, the current I_{Xij} is proportional to x_{ij}. The set of current sources I_U that implement the constant "-1" in Eqs. (10) and (11), are realized with single n-channel MOS transistors operating in subthreshold. The "Lagrange nodes" with capacitance C are pre-charged to V_{DD} before their dynamics take place. Fig. 2 shows the complete circuit diagram of the building block based on the FGMOSFET, where all transistors work in subthreshold.

The circuit of Figure 2, works on subthreshold regime and $Q_{FG} = 0$ and $C_i \gg C_{DS}$ are considered. So, the drain current of M_1 is given by Eq. (10).

$$I_{D1} = I_0 \exp\frac{1}{nv_t}\left(V_{DD} - V_{Sij}\right) \quad (10)$$

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Where V_{Sij} is the input voltage from the cost matrix. The drain current of M_2 is given by Eq. (11).

$$I_{D2} = I_0 \exp\frac{1}{nV_t}\left[\left(\frac{C_{1\_M2}}{C_{T\_M2}}\right)V_1 + \left(\frac{C_{2\_M2}}{C_{T\_M2}}\right)V_{Pi} + \left(\frac{C_{3\_M2}}{C_{T\_M2}}\right)V_{Qj}\right] \quad (11)$$

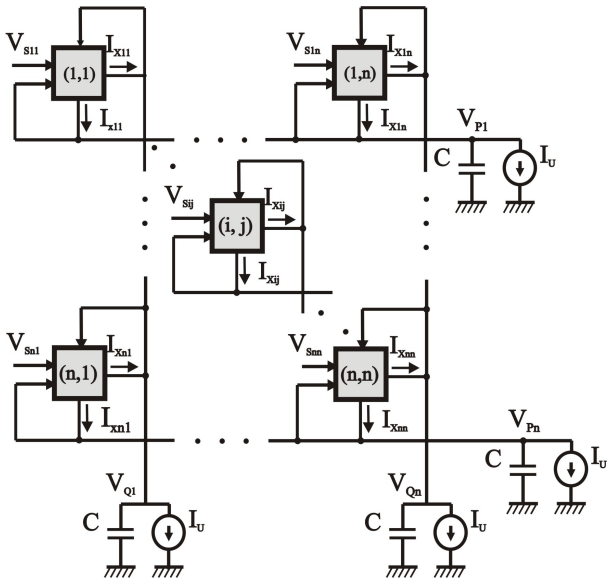

Figure 1. Current-mode array of the analog network that find an optimal solution for the Assignment Problem in current-mode

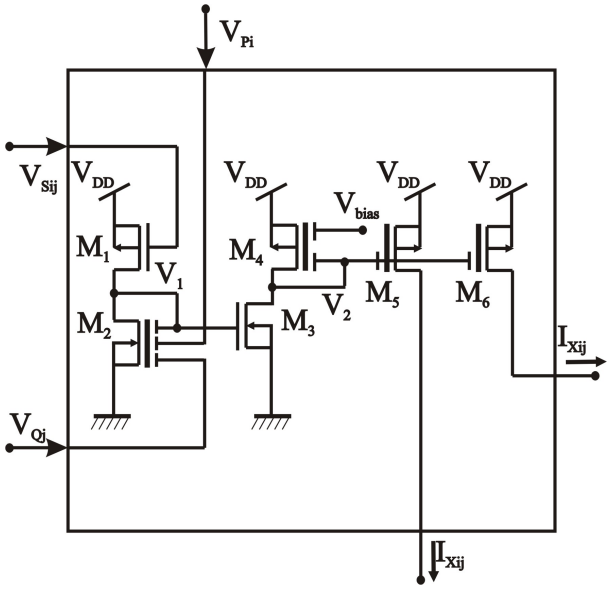

Figure 2. Internal configuration of ij-block

Where C_{T_M2} is the total capacitance, and C_{1_M2}, C_{2_M2} and C_{3_M2} are the input capacitances. By equalizing Eq. (10) with Eq. (11), V_1 is given by Eq. (12).

$$V_1 = \left(\frac{C_{T\_M2}}{C_{1\_M2}}\right)V_{DD} - V_{Pi} - V_{Qj} - \left(\frac{C_{T\_M2}}{C_{1\_M2}}\right)V_{Sij} \quad (12)$$

Following the same procedure as above, the output current I_5 is given by Eq. (13).

$$I_5 = I_{0M5}\exp\frac{1}{nV_t}\left[-\left(\frac{C_{T\_M4}}{C_{2\_M4}}\right)\left(\frac{C_{1\_M5}}{C_{T\_M5}}\right)\left(V_{Pi}+V_{Qj}\right) - \left(\frac{C_{1\_M5}}{C_{T\_M5}}\right)\left(\frac{C_{T\_M4}}{C_{1\_M4}}\right)\left(\frac{C_{T\_M2}}{C_{1\_M2}}\right)V_{Sij} + V_{K2}\right] \quad (13)$$

Where V_{K2} is given by Eq. (14).

$$V_{K2} = V_{DD} - \left(\frac{C_{T\_M4}}{C_{1\_M4}}\right)V_{DD}\left(1 - \left(\frac{C_{T\_M2}}{C_{1\_M2}}\right)\right) + V_{bias} \quad (14)$$

Where the term $\left(\frac{C_{1\_M5}}{C_{T\_M5}}\right)\left(\frac{C_{T\_M4}}{C_{1\_M4}}\right)\left(\frac{C_{T\_M2}}{C_{1\_M2}}\right)$ represents the value of $\frac{1}{T}$.

It must be noticed that V_{Sij} is multiplied by this term, which is indeed always greater than one, ensuring an enough small value of T.

The Hungarian algorithm [7], which is an iterative method used to find the solution of assignment problems, was implemented to compare the real solution with the solution presented by this analog method.

VI. Simulation Results

Several simulations were developed for 2x2, 4x4 and 8x8 matrixes with random values that represent assignment costs; all of them converge to an optimal solution. The supply voltage is 3V. Final simulation using a SPICE Program is presented only for a 4x4 matrix which is given by (15).

$$\begin{pmatrix} 2.16 & 2.165 & 2.18 & 2.175 \\ 2.14 & 2.11 & 2.145 & 2.13 \\ 2.14 & 2.13 & 2.135 & 2.115 \\ 2.165 & 2.15 & 2.11 & 2.15 \end{pmatrix} \quad (15)$$

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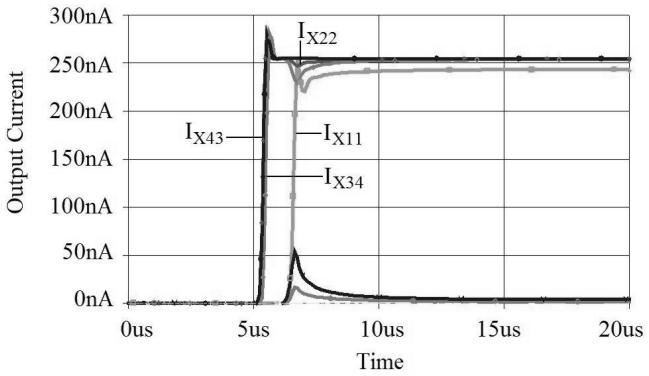

Figure 3. Output currents

Whose solution is obtained through the Hungarian algorithm and is given by (16).

$$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix} \quad (16)$$

Final currents are presented at Fig. 3. Solution currents converge to 250 nA, while non–solution currents converge to 0 nA

The solution is represented by I_{11}, I_{22}, I_{43} and I_{34}, which match with the solution given by the Hungarian algorithm

VI. Conclusions

An analog solution for the assignment problems was proposed in this work. 8x8, 4x4 and 2x2 current-mode arrays were simulated by using a SPICE Program and probed through the Hungarian algorithm. Final simulations probes that the analog network has a good performance on time and also it has low-power consumption by using the advantages of FGMOSFET working on subthreshold regime. It must be noticed that the number of connections increase linearly as the dimension of the cost matrix increases, in comparison with other works, where the number of connections increase in a polynomial way, occupying a greater area on a chip. It should be considered the mismatch effects due to the trapped charge in the floating gate during the fabrication process, in this case, the amount of charge may require to be programmed in order to avoid the mismatch problems, which would affect the circuit performance.

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