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Analysis and measurement of a photo diode used as a control gate in a floating–gate MOS transistor

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ABSTRACT

This paper reports a new operating use regarding the floating–gate MOS transistor (FGMOS). Here it is demonstrated that the typical open circuit voltage (V_{OC}) of a CMOS integrated photo sensor can be coupled to the floating gate of a FGMOS. Several photo sensors structure designs are studied and measured. Results demonstrated that the threshold voltage of the transistor can be modulated optically with a series array of photo sensors to increase the coupled voltage. Therefore, a micro solar cell integrated with a CMOS technology can be used as a control gate giving an optical alternative to modulate the I–V characteristics of a FGMOS, extending the reliability of this device beyond the known injection phenomena commonly used to program it. Also, more than one control gate can be used with only one transistor, giving opportunity to explore the convenience to use this proposal within a pixel design since only one transistor is used, with its floating gate as a summing node.

1. Introduction

One of the devices mostly used in electronic circuits is the Floating–gate MOSFET (FGMOS) since it was first presented by [1] in the late 1960′s. Structure improvements and applications based on this device became an interesting task for researchers and manufacturers regarding the enormous potential that was visualized once the FGMOS was proposed. First, it was mainly used for EEPROM's, EPROM's and Flash Memories within the digital domain of electronics, taking advantage of its non–volatile property to store information. Nevertheless, due to the increasing interest and functionality features that were found for the FGMOS through time, analog and mixed signal applications were reported as well, widening the possibilities to create circuits and systems in areas like artificial neural networks (ANN), analog and mixed signal circuit design, reconfigurable circuits, low voltage–low power implementations, instrumentation amplifiers, etc. A large variety of literature can be found about contributions where the FGMOS was conveniently used, showing the high reliability and functionality that can be achieved [2–5]. Even more, actually it can be found standard CMOS technologies which can offer processes that are very accessible and reliable for prototyping employing FGMOS devices for research purposes, among others. Although it seems that everything is said about the functionalities regarding the FGMOS, it should be remarked that this paper deals with an extension of the properties of this device not yet reported, demonstrating at first instance the hypothesis that the voltage coming from the anode or cathode of a photo sensor, i.e. the open circuit voltage of an integrated photocell, V_{OC}, can be capacitively coupled to the floating gate, and this can give place to attach several photo sensors as control gates, obtaining at the isolated node a weighted sum of the voltage contribution of each photo sensor. This may lead to further proposals of different and simpler configurations of active pixels, for instance, working in voltage mode rather than with integrated photocurrent. Hence, this work can be thought as a preliminary exploration of a FGMOS focused to optical applications, added to that reported, for instance, in [6], where a denominated "*chemical injection*" was used to transfer charge to/from the floating gate, where it is used as a medium of chemical to electrical transduction in a CMOS–MEMS semiconductor gas sensor (SGS). This chemical injection is an alternative to the commonly used electrical charge injection procedures, this is, Fowler–Nordheim tunneling (FNT) or

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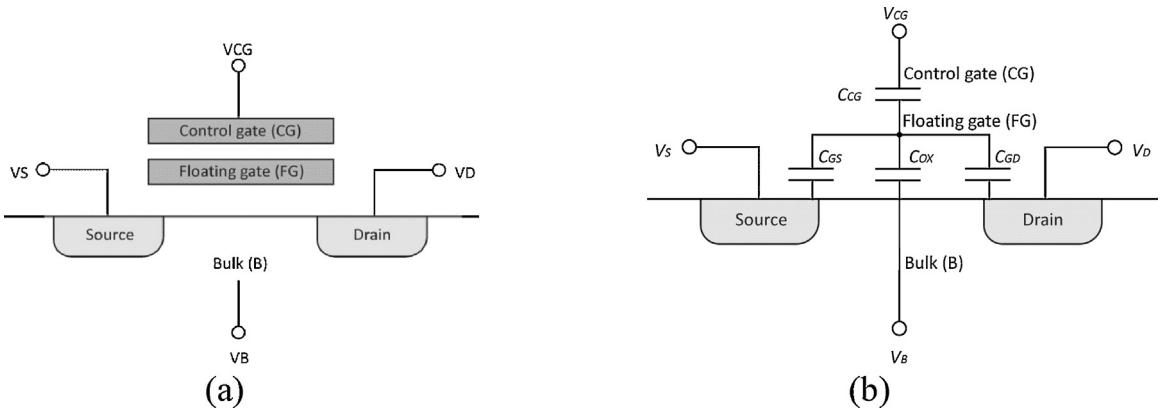


Fig. 1. Structure of a FGMOS. a) Cross section of a FGMOS; b) Capacitive equivalent circuit with one control gate.

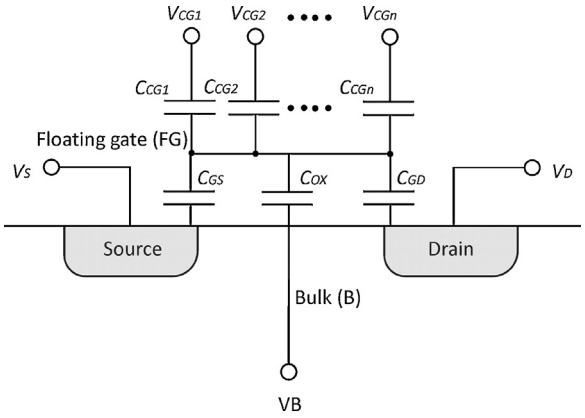


Fig. 2. Capacitive equivalent circuit of a FGMOS with n control gates.

Channel Hot Electrons (CHE) adding an extra functionality to the deviceís performance. This can be possible since chemical reaction or photons, as proposed in this work, can make a voltage to be present over the floating gate as a result of the respective phenomenon, operating this way as a voltammetric sensor. This means that as there is no gate current in a MOSFET, any voltage present upon the gate will define the operation of the device. It should be mentioned that there are several ways to have a voltage present upon the floating gate. Normally, biasing of the gate is made applying an external voltage source to a control gate, coupling it to the floating gate, so a fraction of this applied voltage is present over the floating gate via a coupling capacitor. But on the other hand, there is also the possibility to chemically establish a voltage due to a chemical reaction, where ion charge can be created at the floating gate due to an electrochemical reduction reaction as predicted by the Nernst equation. Furthermore, the open circuit voltage, V_{OC}, of an illuminated photo cell coupled to the floating gate can also drive the I–V characteristics of the FGMOS, being this an optical option, besides the already known electrical methods. By these two means mentioned above, the electrical characteristic of the FGMOS can also be modified and a correlation to physical phenomena, either chemical or photonic, can be established correspondingly. Therefore, here it will be demonstrated that modulation of the I–V characteristics of the FGMOS can be reached via other modes, different from those normally achieved with electrical fields. So, this work covers a use of the FGMOS unexplored until now.

The structure of this paper starts in Section 2 giving some considerations regarding the coupling coefficient of a conventional FGMOS transistor and how it is modified when a photo sensor is added as a control gate to a FGMOS transistor; next the used photo diode structures are commented in Section 3; Section 4 shows the measurement procedures used in this work; Section 5 shows simulations of the response obtained with and without a photo diode connected as a control gate are compared; next, in Section 6 results from optical and I–V characterization are shown; Section 7 includes a brief discussion of the results; and finally Section 8 are the conclusions of this work.

2. Coupling coefficient of a conventional FGMOS

One concept that helps to explain the operation of a FGMOS is based on the coupling coefficient parameter and a short explanation is given next. Obtaining the exact coupling coefficient is a very difficult task and is still in study, as can be seen for instance, in [7–9] and gives rise to issues of modeling theory to correctly simulate the current–voltage characteristics of the FGMOS that are still in discussion. A complete treatise on this matter can be found in [10], where special attention is focused over the different circumstances that can affect the accuracy in the calculation of the coupling coefficient. Fig. 1(a) shows a simple representation of a Floating–gate MOSFET, where it can be seen that it is similar to a conventional MOS transistor, but with an extra gate embedded within silicon dioxide, called "*Floating Gate* (*FG*)". Therefore, this extra gate has no electrical connection, so it is electrically floating. The gate above the *FG* is named "*Control Gate* (*CG*)" and is where the gate voltage, V_{GS}, is applied to bias the transistor according to the desired operating regime, together with the voltage applied to the drain terminal, V_{DS}. There, V_S and V_B are the voltages at Source and Bulk, respectively, and regularly are equal to zero. Obviously if V_S and V_B are not zero, the corresponding terms in eq. (6) will be summed to the final V_{FG}. According to [10], Fig. 1(b) shows the capacitive equivalent circuit, where, C_{CG}, C_{OX}, C_{GD} and C_{GS} represent the capacitances between control gate and floating gate, floating gate and bulk, floating gate and drain, and floating gate and source, respectively. The concept of "*coupling coefficient, K_{CG}*" for a conventional FGMOS is defined taking into account these elements, as follows:

$$K_{CG} = \frac{C_{CG}}{C_T} \tag{1}$$

$$K_B = \frac{C_{OX}}{C_T} \tag{2}$$

$$K_{GD} = \frac{C_{GD}}{C_T} \tag{3}$$

$$K_{GS} = \frac{C_{GS}}{C_T} \tag{4}$$

Where:

$$C_T = C_{CG} + C_{OX} + C_{GD} + C_{GS} \tag{5}$$

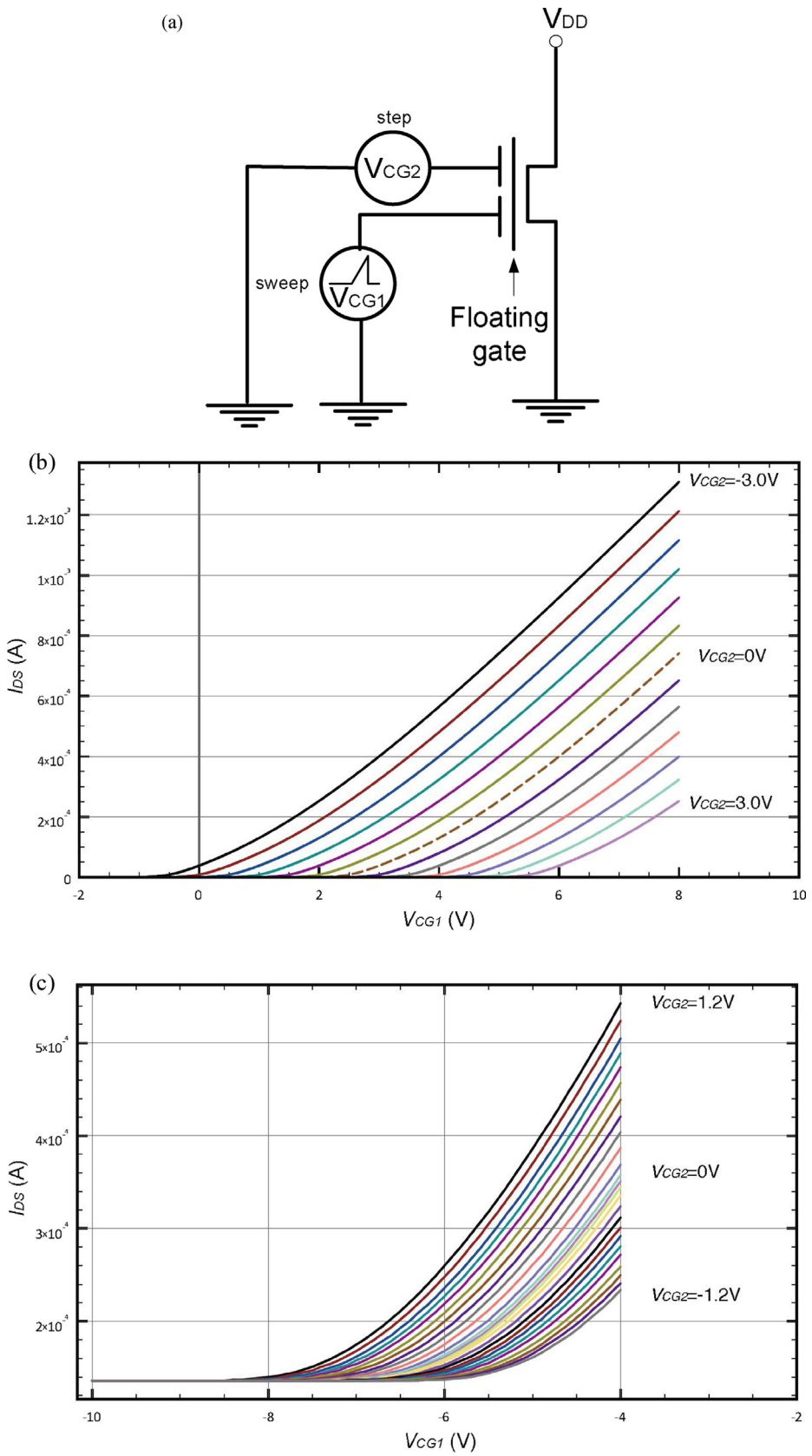


Fig. 3. Transconductance plot of a N–channel FGMOS with two control gates. a) measurement and simulation set; b) simulation results; c) experimental results.

Next, the voltage present upon the floating gate, V_{FG}, can be calculated with (6) [10]:

$$V_{FG} = K_{CG}V_{CG} + K_{OX}V_B + K_{GD}V_D + K_{GS}V_S \quad (6)$$

From (6) it can be seen that the floating gate voltage, V_{FG}, is a sum of the fraction of the voltage applied to each terminal and it is important to highlight that the terms expressed in (1)–(4) are fixed and

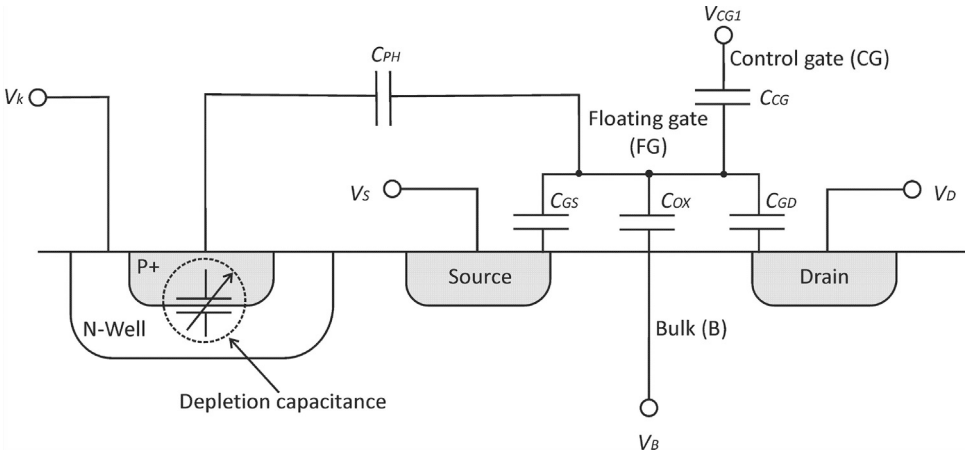


Fig. 4. Schematic diagram of the structure FGMOS-photo sensor.

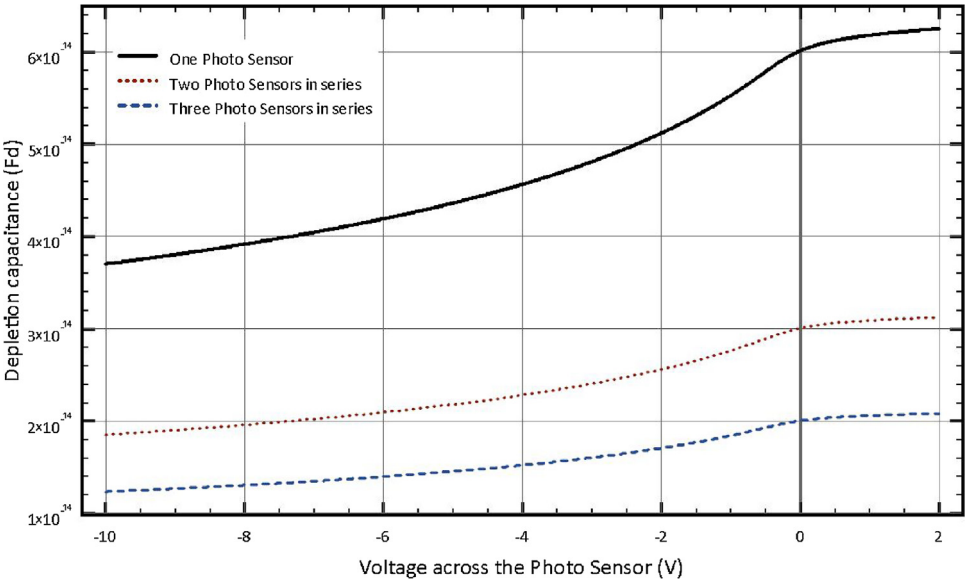


Fig. 5. Depletion capacitance variation of one photo sensor, two photo sensors connected in series, and three photo sensors in series.

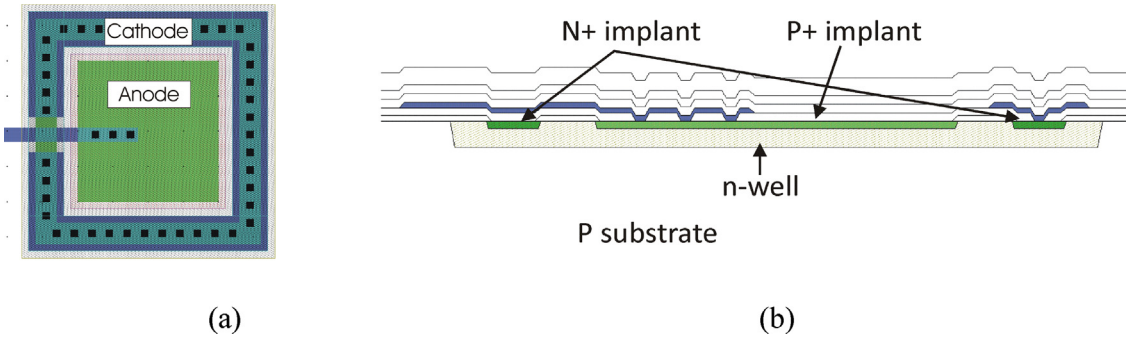


Fig. 6. a) Layout of the photo diode; b) cross section of the p+/n–well structure of the photo diode.

that V_{FG} will be a function only of V_{CG}. This is the case for a FGMOS with only one control gate, but there can be n control gates, as is shown in Fig. 2. In this late case, the coupling coefficient with its respective applied voltage is used together to obtain V_{FG}, with $K_{CG1}V_{CG1}, K_{CG2}V_{CG2}, \ldots, K_{CGn}V_{CGn}$ added to (6). Moreover, to consider the possibility of the existence of residual charge, Q_{FG}, due to technological processes over the floating gate, Eq. (6) must be rewritten to include this charge, as shown in (7).

$$V_{FG} = K_{CG1}V_{CG1} + K_{CG2}V_{CG2} + \ldots + K_{CGn}V_{CGn} + K_{OX}V_B + K_{GD}V_D + K_{GS}V_S + \frac{Q_{FG}}{C_T} \quad (7)$$

Fig. 3(a) shows the set used in a simulation of a N–channel FGMOS with two control gates, V_{CG1} and V_{CG2}, where a voltage

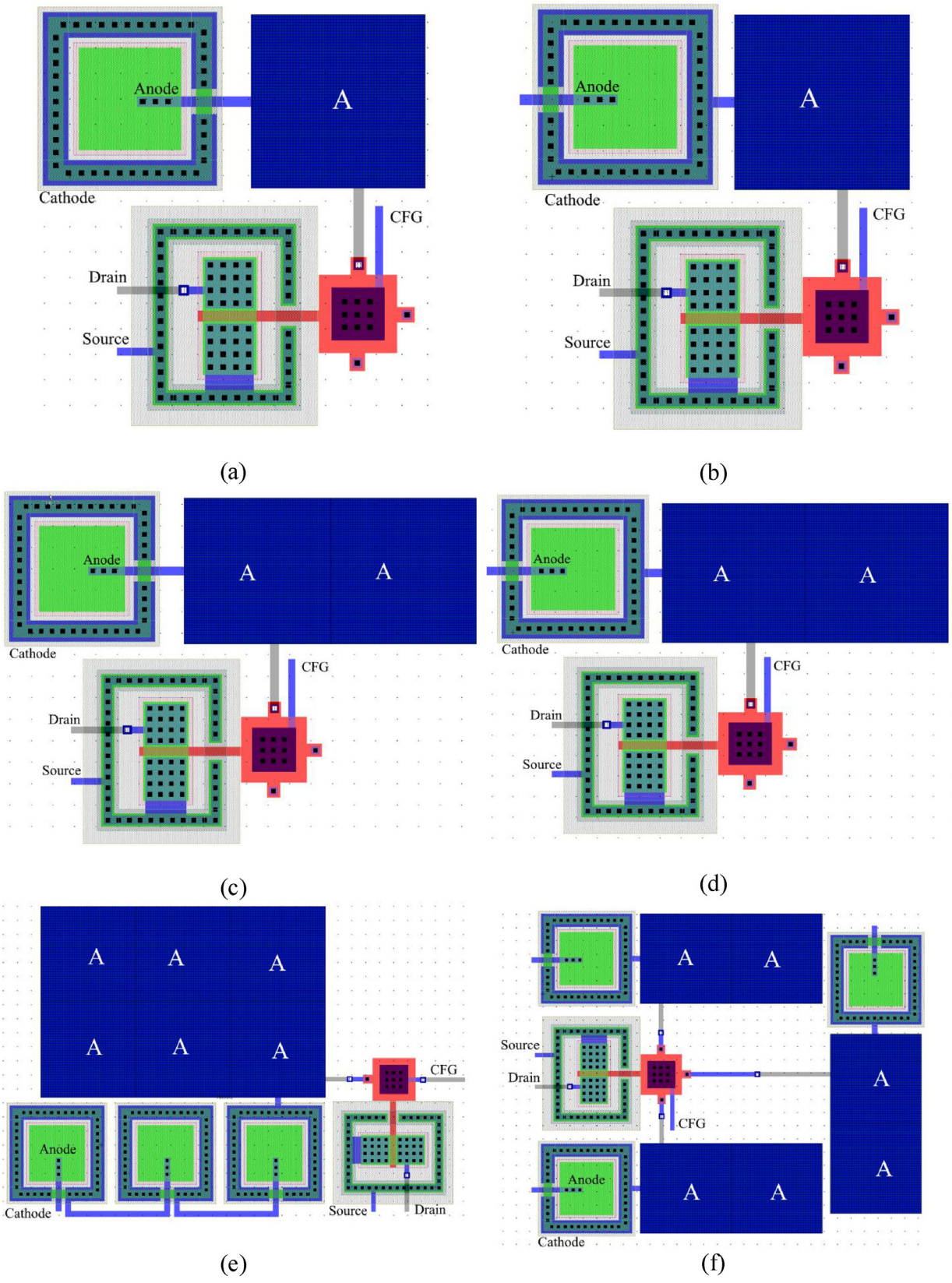


Fig. 7. a) Single diode with its anode connected to a coupling capacitor with area A; b) Single diode with its cathode connected to a coupling capacitor with area A; c) Single diode with its anode connected to a coupling capacitor with area 2A; d) Single diode with its cathode connected to a coupling capacitor with area 2A; e) Three diodes series array with cathode connected to a coupling capacitor with area 6A; f) Three diodes parallel array with cathode connected to a coupling capacitor with area 2A.

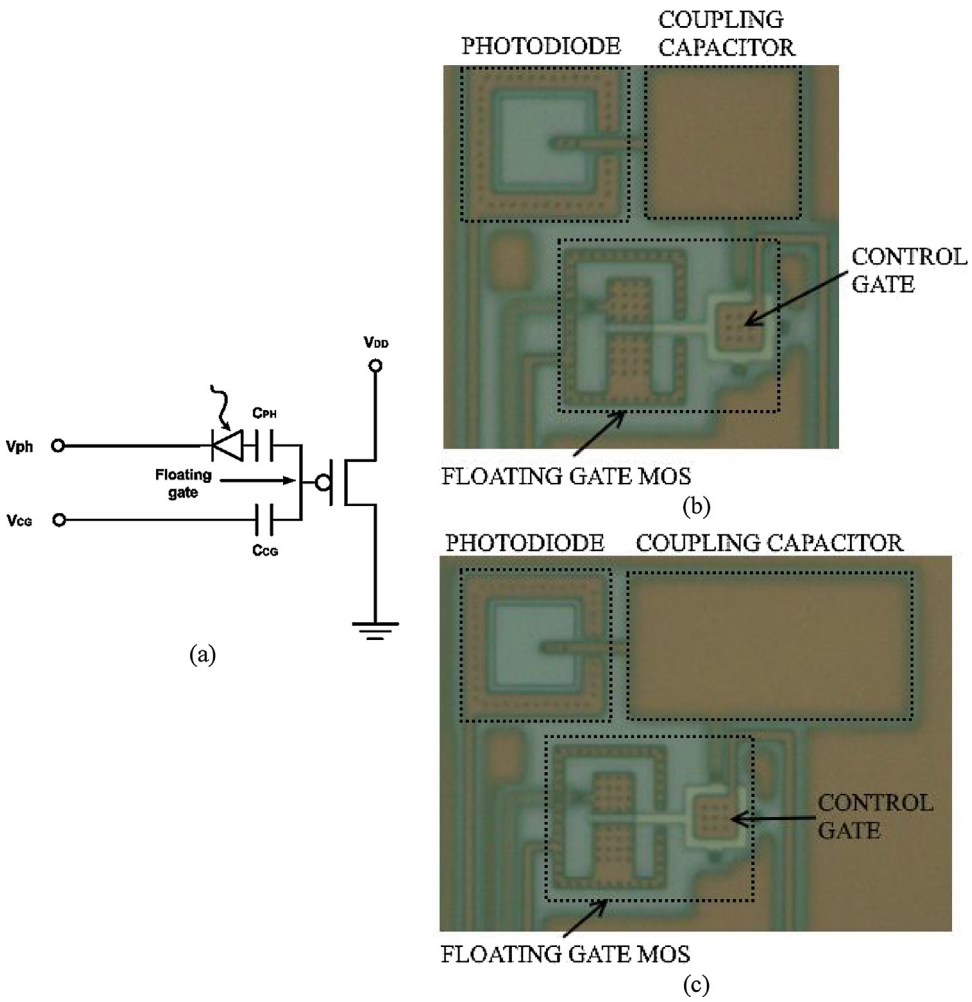


Fig. 8. Single diode with its anode connected to a coupling capacitor; a) schematic; b) with area A; c) with area 2A (A = 20.4 μm × 20.4 μm)).

sweep to V_{CG1} is made from −2 V to 8 V, with V_{CG2} as parameter with 0.5 V steps with V_{DD} = 5 V to assure that the device operates in saturation. Fig. 3(b) shows the simulation results. Voltages on both control gates are applied externally and are coupled to the floating gate. As it can be seen, in the I_{DS} vs V_{CG1} plot, a family of curves is derived due to the sum of the coupled voltages over the floating gate for each value of V_{CG2}, as predicted by Eq. (7). This is confirmed experimentally in Fig. 3(c) after a N–FGMOS with two control gates was measured. Here, external voltage sources were used to bias the transistor the same way in which simulation was done. The reason why the plot is shifted to the left in this late case is because residual positive charge due to technological processes is present over the floating gate. The polarity and magnitude of this charge is random and it can be reduced or eliminated if the device is illuminated with UV light. The curves should be shifted to the right if this random charge is negative. Besides, from Eq. (7) it should be clear that despite the number of control gates present in the FGMOS design, V_{FG} is always a fraction of the sum of the voltages applied to all control gates. Therefore, as the transconductance graph of this device plots the drain current as a function of V_{CG1}, the apparent threshold voltage $V_{TH}{}^{*}$ that can be obtained from this plot, is always different from the native threshold voltage V_{TH} of the embedded MOS transistor (this V_{TH} can be deduced if I_{DS} is plotted as a function of V_{FG}), independently of the nature and conditions of the voltage present at each control gate V_{CGn}.

From Fig. 3 it can be seen that the floating gate of a FGMOS plays the role of a summing node of weighted voltages coming from the control gates. Therefore, as it is intended to being demonstrated in this paper, a voltage due to any nature present in a control gate can be partially reflected over the floating gate due the coupling coefficient, modulating in consequence the I–V characteristics of the FGMOS. Hence, it is important to remark that the work here presented shows that this voltage is different from those already reported.

2.1. Floating gate voltage with a photo diode as control gate

It should be remembered that the purpose of this paper does not deal strictly with the several aspects concerning the coupling coefficient as is addressed in [10], but rather to point out the behavior that it has when a photo sensor is part of the control gate and to show how the I–V characteristics of the FGMOS respond depending on the voltage connected to one of the available terminals of the photo sensor. Also, it is important to first remark that the main goal of this work is to demonstrate that one terminal of the photo diode (either anode or cathode) can operate as the plate of a coupling capacitor, such that a weighted voltage coming from the photo diode can be present on the floating gate of a FGMOS. This will be a different way in which coupling is normally made, since usually a simple and fixed coupling capacitor is connected directly to the signal line or node, without any intermediary device, as this proposal will show, since in this case the associated capacitance of a photo diode (even directly or inversely biased) is used as the coupling capacitor being a different alternative. This case can be addressed

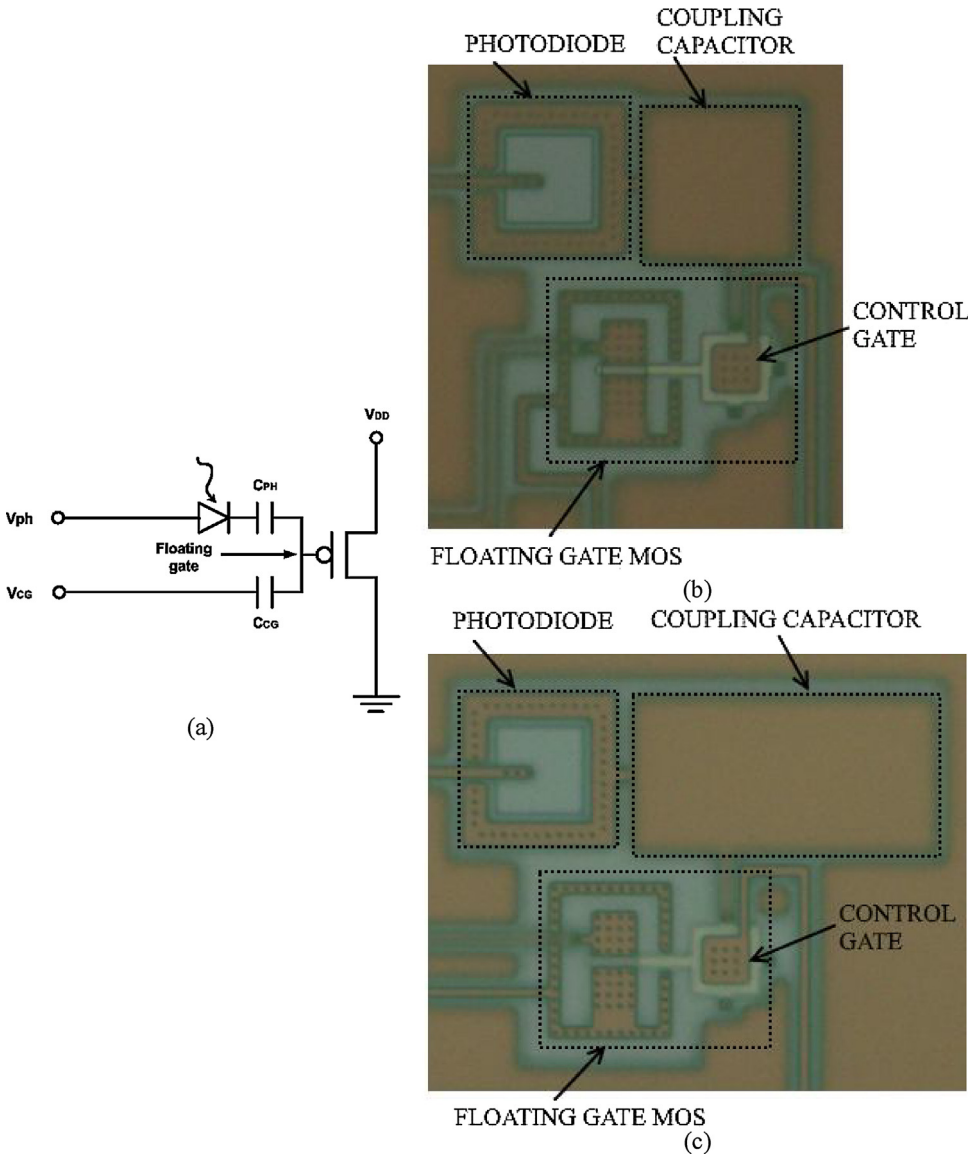


Fig. 9. Single diode with its cathode connected to a coupling capacitor a) schematic; b) with area A; c) with area 2A (A = 20.4 μm × 20.4 μm)).

considering in Eq. (7) the depletion capacitance of the *p-n* junction used configured as a photo diode. Therefore, for a FGMOS with two control gates, K_{CG1} in (7) can be expressed as follows when a photo sensor is placed as a control gate:

$$K_{CG1} = \frac{C_j}{C_T} \tag{8}$$

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_D}{\phi_0}\right)^m} \tag{9}$$

$$\varphi_0 = V_T \cdot \ln\left(\frac{N_a \cdot N_d}{{n_i}^2}\right) \tag{10}$$

where:

C_{j0}: zero-bias depletion capacitance of a *p-n* junction (Fd/m^2)
V_D: voltage across the *p-n* junction (V)
ϕ_0: built in potential (V)
m: grading coefficient
V_T: thermal voltage (V)
N_a: acceptor concentration (cm^{-3})
N_d: donor concentration (cm^{-3})
n_i: intrinsic concentration (cm^{-3})

Additionally, total capacitance for the structure shown in Fig. 4 is expressed as follows:

$$C_T = \frac{C_j \cdot C_{PH}}{C_j + C_{PH}} + C_{CG} + C_{OX} + C_{GS} + C_{GD} \tag{11}$$

Finally, regarding the structure shown in Fig. 4, the expression to find the voltage over the floating gate of a FGMOS with two control gates, where one of them is a photo diode, can be written as follows:

$$V_{FG} = \frac{C_j \cdot C_{PH}}{C_T\left(C_j + C_{PH}\right)} V_K + \frac{C_{CG}}{C_T} V_{CG1} + \frac{C_{OX}}{C_T} V_B + \frac{C_{GD}}{C_T} V_D + \frac{C_{GS}}{C_T} V_S + \frac{Q_{FG}}{C_T} \tag{12}$$

From (12) it can be seen that V_{FG} is now a function of C_j, which in turn is a function of the voltage applied to the *p-n* junction of the photo diode (see Eq. (9)) and since the other terms in (12) are fixed, V_{FG} will follow the variations in the depletion capacitance of the photo diode junction. This is assessed through simulations and experimental measurements shown in the next sections. Fig. 4

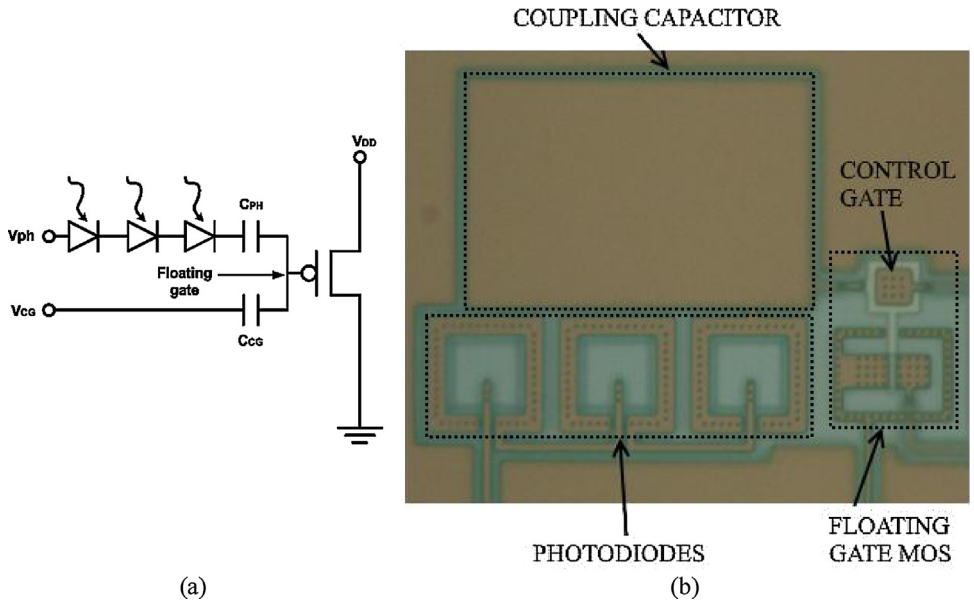


Fig. 10. Three diodes series array with cathode connected to a coupling capacitor with area 6A; a) schematic; b) photograph.

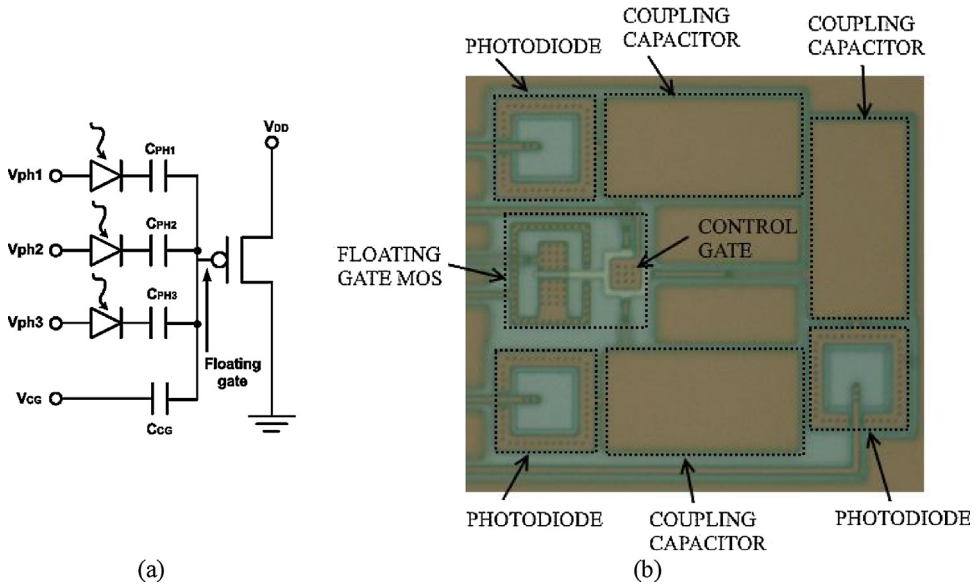


Fig. 11. Three diodes parallel array with cathode connected to coupling capacitors with area 2A each; a) schematic; b) photograph.

shows a schematic diagram of the structure FGMOS-photo sensor, where the elements considered for simulation are considered.

The set used for simulation and experimental measurements is described following. The voltage applied to the control gate, V_K, (the terminal of the photo diode in this case) is different from the power supply voltage, V_{DS} and V_{CG}. The purpose of the gate voltage applied to the photo diode is mainly to establish a reverse bias to the junction presenting a depletion capacitance whose value is a function of the applied voltage. This is what will give the feature to the FGMOS of a variable coupling coefficient instead of the one that is normally designed with a fixed capacitance. In this condition, once the photo sensor is illuminated typical parameters for this device are present, like *Short Circuit Current*, I_{SC}, and *Open Circuit Voltage*, V_{OC}. This last voltage is the one that is used to be coupled to the floating gate in this study, using series or parallel arrays of photo sensors. Then, once the behavior is analyzed a decision has to be made if the photo diode should be forward (maximum depletion capacitance) or reverse biased (variable capacitance depending on the applied voltage magnitude) upon the behavior desired. On the other hand, it is demonstrated that the coupling capacitance will not be the same in each case (forward or reverse bias) and this will lead the floating gate to have a different voltage for each polarity, thus presenting a different trending from what is obtained with traditional methods, where coupling coefficient is fixed when a structure like a photo diode is not included as a control gate. In other words, this coupling capacitance is a function of the voltage drop across the photo diode, as is shown in (8) and (11). On the other hand, biasing of the FGMOS with a supply voltage, V_{DS}, and the second gate voltage, V_{CG}, is strictly to establish the operation regime of the MOS transistor, named linear or saturation. Therefore, V_{DS} and V_{CG} are used to set the FGMOS to an operating point and V_K is used to forward or reverse biasing of the photo diode to create electron-hole pairs once illuminated, from which the open circuit voltage, V_{OC}, is derived. Besides, it should be remembered that the main purpose of this paper is to demonstrate that the voltage due to the illumination of a photo diode can also be detected and coupled to a FGMOS.

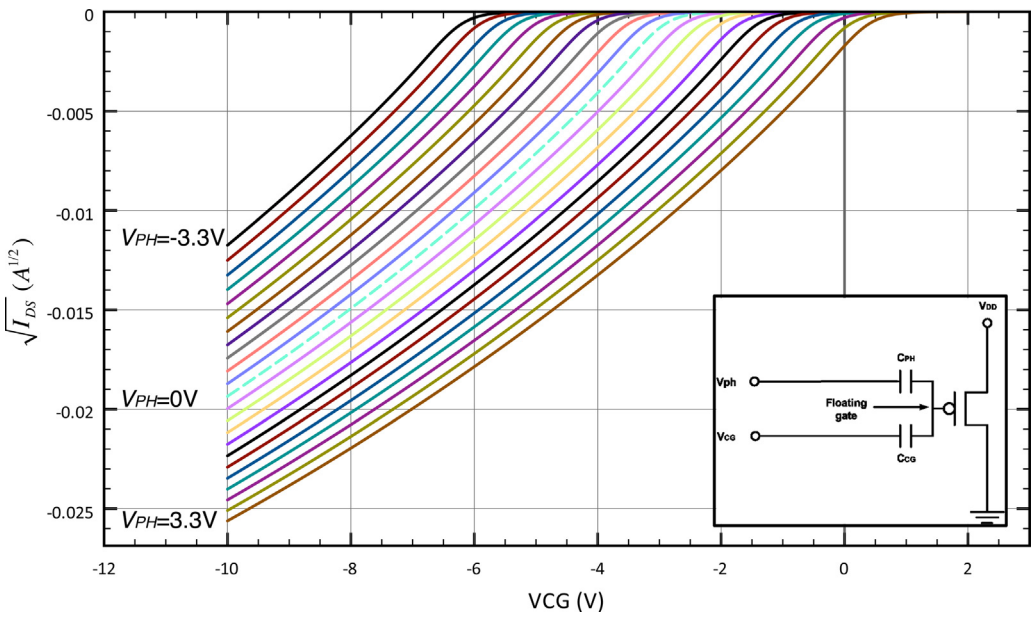


Fig. 12. Plot of $\sqrt{I_{DS}}$ vs V_{CG} with the coupling capacitor C_{PH} having an area of 2A. Dashed line corresponds to V_{PH} = 0 V.

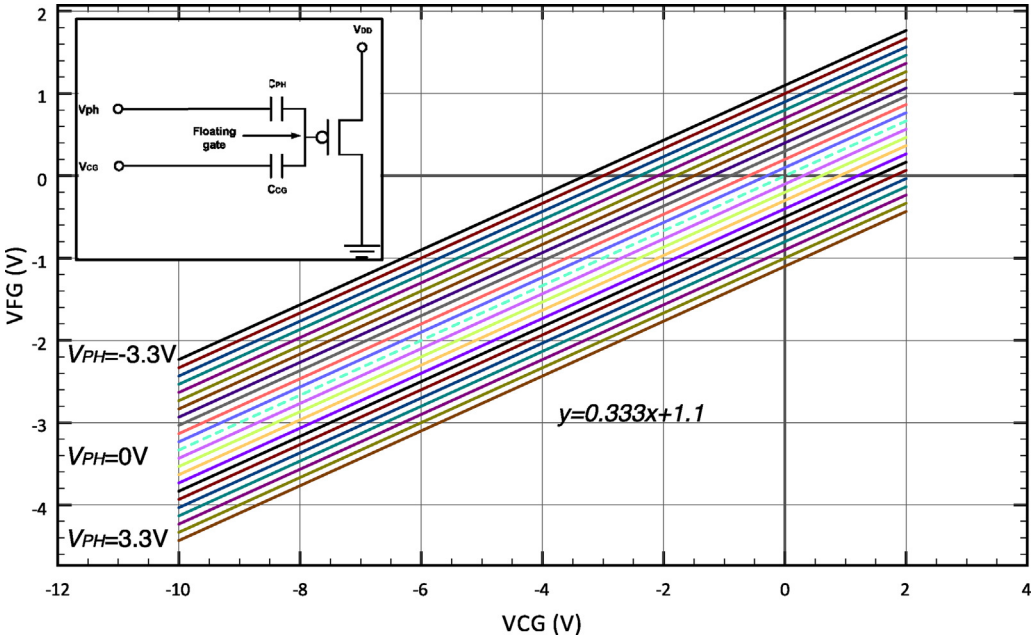


Fig. 13. Plot of V_{FG} vs V_{CG} with the coupling capacitor C_{PH} having an area of 2A. Dashed line corresponds to V_{PH} = 0 V.

This method together with that reported in [6] are different from traditional electrical methods like Fowler-Nordheim tunneling and Channel Hot Electrons. Also it is important to say that the chemical injection can give to the gas sensor reported in [6] represents a non-volatile feature, whereas the method here reported represents a volatile feature to the FGMOS.

2.1.1. Depletion capacitance of the photo diode

Using Eq. (9) with the technological parameters of the AMI 0.5 μm process and the geometry of the photo sensor described in Section 3, a simulation was carried out to show the variation range of the depletion capacitance. Besides, since it is connected in series with the coupling capacitance made with aluminum, its variation will strongly influence the resulting capacitance because it is smaller than the coupling capacitance. Fig. 5 shows the variation range of depletion capacitance for one photo sensor, two photo sensors connected in series, and three photo sensors connected in series.

From Fig. 5 it was found that for a reverse bias of −1.8 V of a single photo sensor with the geometry described in Section 3, the depletion capacitance is Cd = 51.755fF and Cd = 62.509fF for a forward bias of 2 V. For the same bias values, the corresponding values for two photo sensors in series Cd = 25.955fF and Cd = 31.255fF, and for three photo sensors in series Cd = 17.304fF and Cd = 20.836fF. Therefore, it is intended to find the influence of the size of coupling capacitance connected in series with the photo sensor, such that an optimum area can be defined for the structure FGMOS-photo diode. Hence, three sizes were proposed for this purpose: a capacitance with a unit area A = 416 μm^2, a capacitance with an area 2A and a capacitance with area 6A.

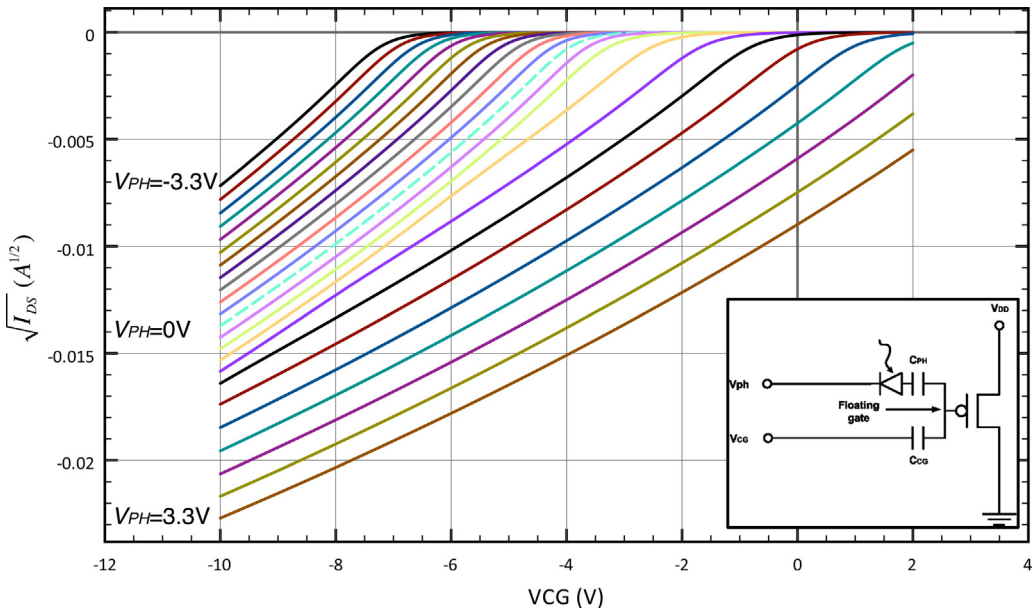


Fig. 14. Plot of $\sqrt{I_{DS}}$ vs V_{CG} with the anode of a photo diode connected to the coupling capacitor C_{PH} having an area of 2A. Dashed line corresponds to V_{PH} = 0 V.

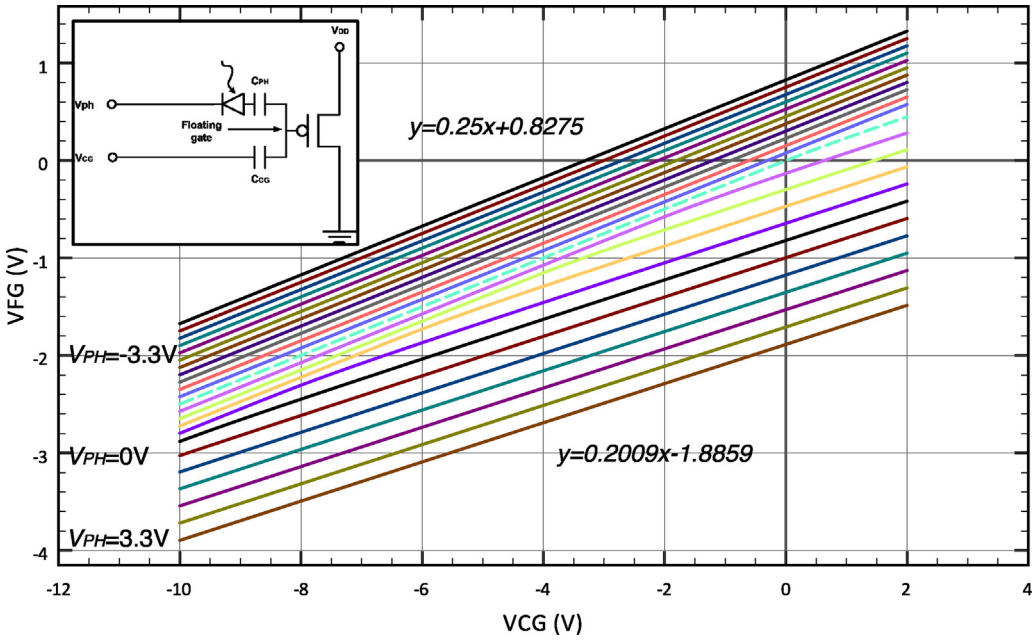


Fig. 15. Plot of V_{FG} vs V_{CG} with the anode of a photo diode connected to the coupling capacitor C_{PH} having an area of 2A. Dashed line corresponds to V_{PH} = 0 V.

3. Outline of the basic structures

A prototype chip was fabricated with a 0.5 μm, N–well, two poly layers, and three metal layers CMOS technology from On Semiconductor. With this process, there is the possibility to integrate photo transistors or photo diodes, as well as floating–gate MOS transistors. Since the study presented in this report has no antecedents, the structures used has an exploration purpose in order to establish some elements that can drive to deeper studies in future works. The six proposed configurations have the following goals: first, verify the response of anode or cathode coupling to the floating gate; next, establish the effect of different coupling capacitors in the behavior of the FGMOS; and last, test the performance of the FGMOS when the input coupling is in series or in parallel. Criteria for the definition of the structures used are now commented. First, based on the results presented in [11–13], it was decided to integrate a photo diode with a p+/n–well structure, as shown in Fig. 4. The area of the anode is 12 μm × 12 μm and the area of the cathode is 21.6 μm × 21.6 μm, which are defined by minimum area photo diodes following design rules restrictions and to achieve a convenient depletion capacitance variation range. Contact to the anode node was minimized to allow maximum illumination through the p–n junction. Since the coupling coefficient is defined in terms of capacitances, three kinds of capacitances can be identified over the design of the structure studied: a) depletion capacitance, b) coupling capacitance, and c) parasitic capacitance. These are defined by technological parameters like implantation contamination, area capacitance between both polysilicon layers, and finally, area and fringe capacitance between polysilicon layer and substrate or channel region and between metal layers and substrate, respectively.

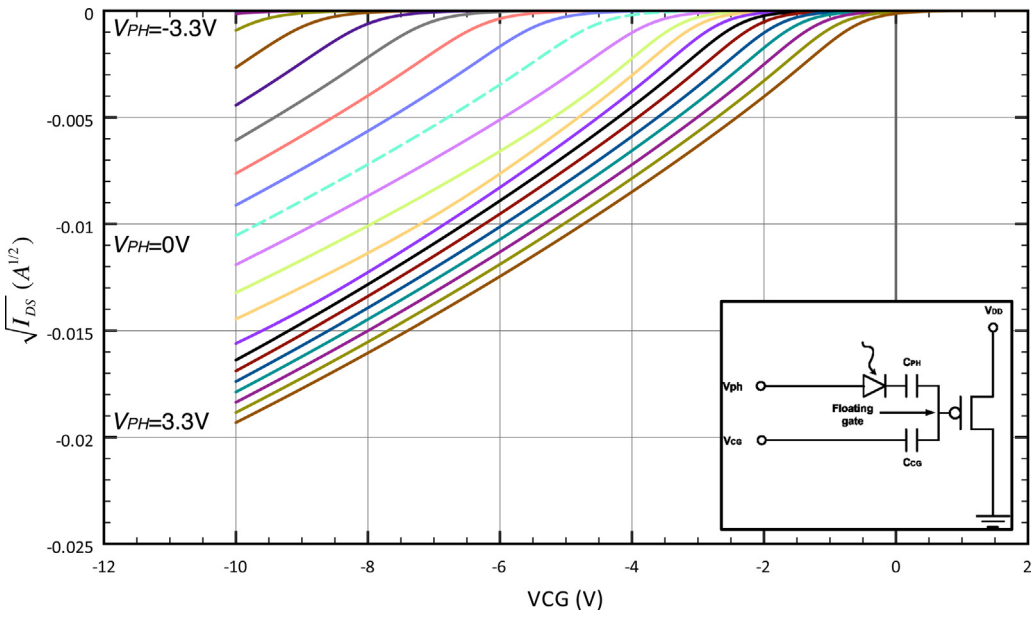


Fig. 16. Plot of $\sqrt{I_{DS}}$ vs V_{CG} with the cathode of a photo diode connected to the coupling capacitor C_{PH} having an area of 2A.

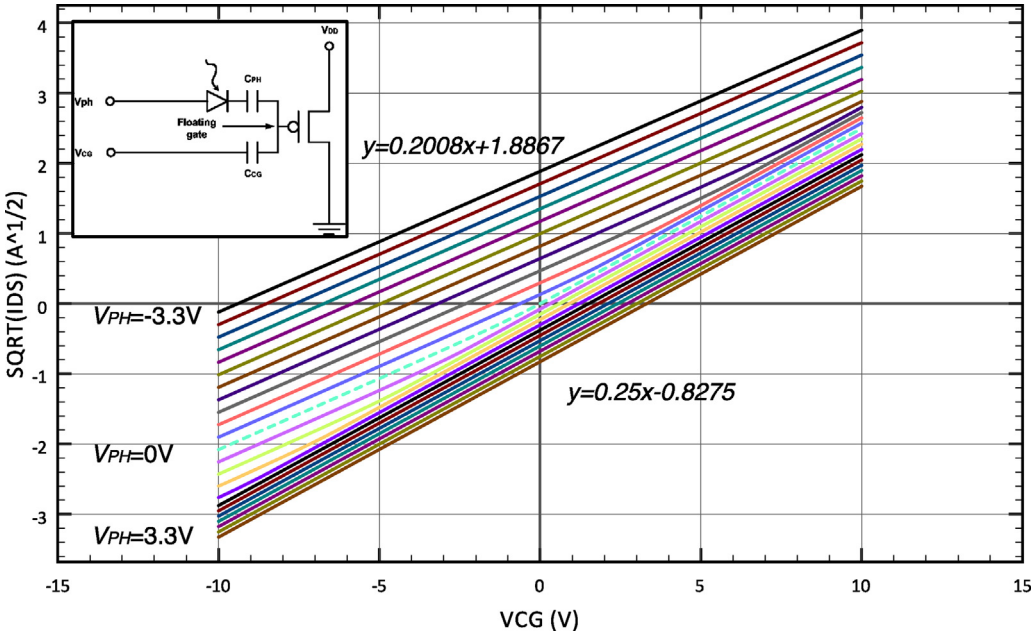


Fig. 17. Plot of V_{FG} vs V_{CG} with the cathode of a photo diode connected to the coupling capacitor C_{PH} having an area of 2A.

For instance, the coupling capacitance made with Poly2 and Poly1 is smaller than the coupling capacitance made with Metal1 and Metal 2 since separation between these two layers is shorter. Talking about the coupling coefficient, it is clear from Eq. (1) that a small coupling capacitance will give a small coupling coefficient and on the other side, a large coupling capacitance will give a large coupling coefficient. Then, regarding the coupling capacitance connected in series with the depletion capacitance, it was decided to use three different areas to evaluate the effects that can be present having a small, medium and large coupling capacitance, but also trying to fit a trade-off between functionality of the FGMOS-photo sensor structure and integration area. With this in mind, coupling coefficients will range between 0.2 and 0.8 and it is expected that valuable information can be obtained regarding the use of a photo sensor as a control gate in a FGMOS.

Furthermore, several arrays of photo diodes were used as control gates in order to test parallel and series arrays as are used in solar cell modules. Although it is clear that there will be no gate current if the photo diode is capacitively coupled to the floating gate, it seems interesting to find out how these arrays reflect over the floating–gate voltage, modifying therefore the I–V characteristics of the FGMOS.

According to these objectives, the proposed configurations used in this prototype chip are described next and are shown in Fig. 5(a)–(f).

1. Single diode with its anode connected to a coupling capacitor with area A
2. Single diode with its cathode connected to a coupling capacitor with area A

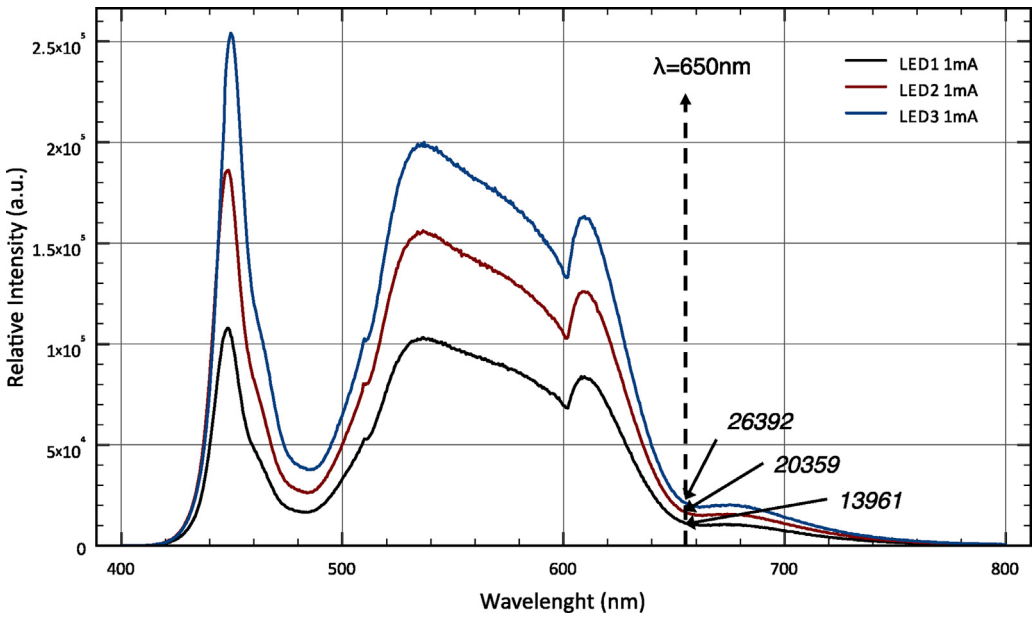


Fig. 18. Photoluminiscense of the ultrabright white LED, VLHW5100.

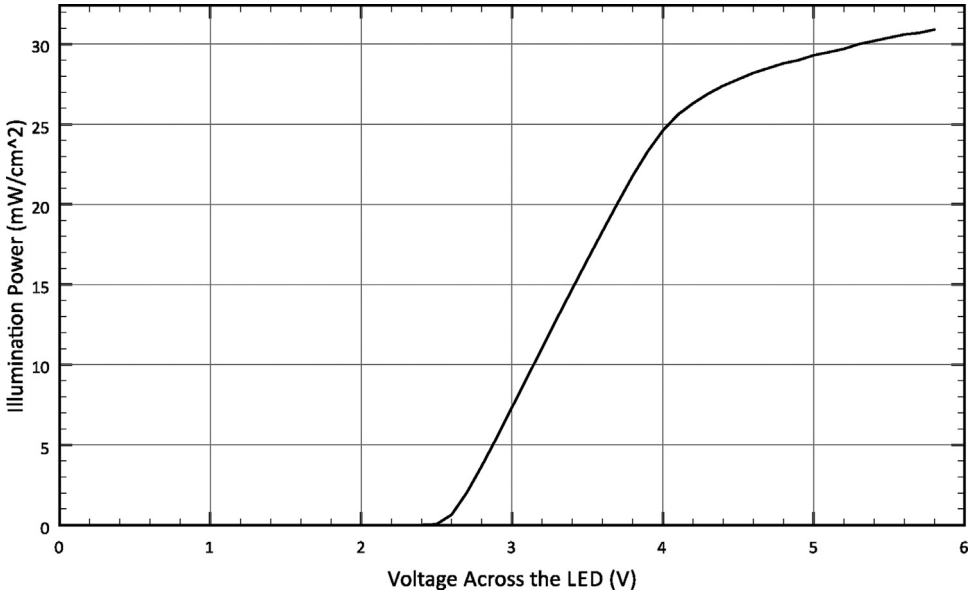


Fig. 19. Optical power of the ultrabright LED as a function of applied voltage.

3. Single diode with its anode connected to a coupling capacitor with area 2A
4. Single diode with its cathode connected to a coupling capacitor with area 2A
5. Three diodes series array with cathode connected to a coupling capacitor with area 6A
6. Three diodes parallel array with cathode connected to a coupling capacitor with area 2A

The layout and cross section of the photo sensor is shown in Fig. 6 and layouts of these six cells are shown in Fig. 7, where the coupling capacitor of these six cells consists of a lower plate made with metal 1 and the upper plate made with metal 2 with a unit capacitor area A = 20.4 μm × 20.4 μm. Using the technological parameters given by the technology, this area delivers an approximate capacitance value of 28.3fF. This coupling capacitor is connected to the floating gate layer of poly,1, connecting metal 2 to metal 1 with the help of a via layer. The control gate coupling capacitor, where V_{CG} is applied, has an area of 6.15 μm × 6.15 μm with a capacitance value of 33.32fF. Finally, the FGMOS used was a p–MOS with L = 1.2 μm and W = 6.3 μm. This size of the FGMOS transistor helps to achieve a trade-off among the area used by the photo diode together with the coupling capacitors and the current delivered by the FGMOS, such that the integration area of the structure can be of minimal size but delivering at the same time a reliable current when it is characterized. The anode is kept also with only one metallic contact to allow for maximum light collecting. Also, using a p–MOS may prevent undesired cross–talk substrate currents since if an n–MOS was used, the p–substrate could set a parasitic diode with the n–well of the photo diode.

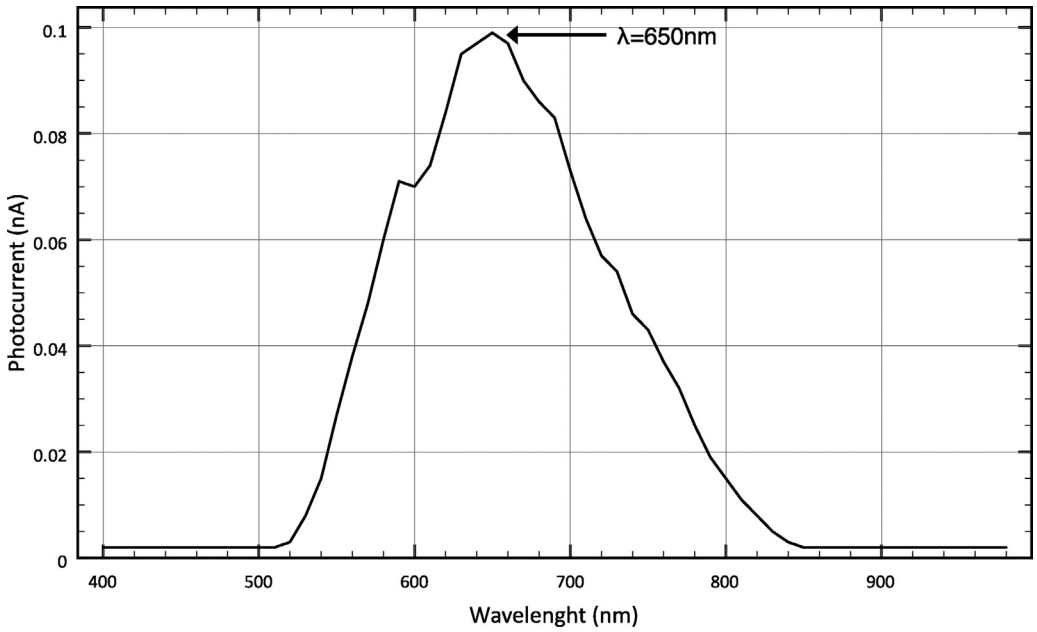


Fig. 20. Photoresponse of the p+/n–well photo diode, Photocurrent vs. wavelength.

4. Characterization procedure

As mentioned before, there are six different test cells to be characterized with four accessing terminals in each cell that can be used for electrical characterization: one for VDD, one for GND, one to bias the control gate with V_{CG} and the last one to bias one terminal of the photo diode, V_{PH}. Figs. 8–11 show the schematics of the circuits that were measured together with the photographs of the integrated photo diode arrays taken with an optical microscope. Only four variations are shown with respect to what is presented in Fig. 7, since Fig. 7(a) and (c) are similar to Fig. 7(b) and (d), respectively, with the only difference in the coupling capacitor area. V_{CG} is the voltage applied to control gate, V_{PH} is the voltage applied to the photo sensor, C_{CG} is the coupling capacitor (fixed area in all the configurations) for control gate and C_{PH} is the coupling capacitor (different area depending on the configuration) connected to the photo sensor.

5. Simulations

In order to have a reference to compare the behavior between cells with and without a photo diode, results from a group of simulations will be presented. Obviously, direct experimental measurement of the floating gate voltage is not possible, so a way to estimate the approximate magnitude of V_{FG} is by means of simulations. From these, it might be clear the role played by the photo diode in each kind of structure. At first instance, it will be shown how the I–V characteristics of a FGMOS are, as well as the evolution of the floating gate voltage when a voltage sweep is applied to the control gate, with the voltage applied to the photo sensor as a parametric voltage step.

5.1. Cell without a photo sensor

A simulation with PSPICE was done, using the technologic and geometric parameters for the coupling capacitors (C_{CG} and C_{PH}) connected to the FGMOS presented before, and particularly, this is a FGMOS with two control gates. V_{CG} was programmed as a voltage sweep from −10 V to 10 V, and V_{PH} was programmed as a voltage step, from −3.3 V to 3.3 V with 0.3 V steps. The FGMOS was biased with V_{DD} = −3.3 V. Fig. 12 shows the transconductance I–V plot for $I_{DS}{}^{1/2}$ vs V_{CG}, where no residual charge was considered over the floating gate, this is, Q_{FG} = 0, and on the other hand, Fig. 13 shows the behavior of V_{FG} with this structure.

From Fig. 12 it can be highlighted the regularity in the separation of the curve set since each curve is shifted by the same value of 0.3 V, following the step value for V_{FG} indicated in PSPICE. This indicates also that the threshold voltage of the FGMOS goes from positive to negative values when V_{PH} goes from negative to positive values, as is expected. This is because when a positive voltage due to V_{PH} is reflected over the floating gate, then V_{CG} has to be more negative to create the inverted channel between Source and Drain to allow I_{DS} current flow. On the other side, from Fig. 13 it can be seen also that V_{FG} has the same slope along the voltage steps used, with a value of 0.3333, which can be considered as an approximate value of K_{CG}. The equation shown in Fig. 13 corresponds to the trend line for V_{FG} vs V_{CG} when V_{PH} = −3.3 V. As a quick reference, the dashed line corresponds to V_{PH} = 0 V.

5.2. Cell with a photo sensor

Next, a simulation was made considering a structure adding a photo diode in the branch of one of the control gates, using the same simulation parameters for V_{DD}, V_{CG} and V_{PH} as before. Fig. 14 shows the results of the simulation, first when the anode is connected to the coupling capacitor having an area equal to 2A, as shown in the figure inset. Again, the transconductance plot is presented as $I_{DS}{}^{1/2}$ vs V_{CG}. The corresponding plot for the behavior of V_{FG} is also presented in Fig. 15.

From Fig. 14 it immediately rises the difference with the uniformity of the response compared with that shown in Fig. 12, and two behaviors can be identified. First, approximately when V_{PH} > 0.6 V the curves have a separation among them ranging from 0.79 V when V_{PH} = 1.2 V, up to 0.89 V when V_{PH} = 3.3 V. This range establishes a reverse bias for the photo diode since a positive voltage is being applied to the cathode. Second, when V_{PH} < 0.6 V, going though negative V_{PH} voltages, the diode is forward biased and it can be considered that C_{PH} is receiving almost all the voltage applied in V_{PH}. This can be confirmed with Fig. 15, where two slopes can be identified within these two behaviors mentioned before. When the

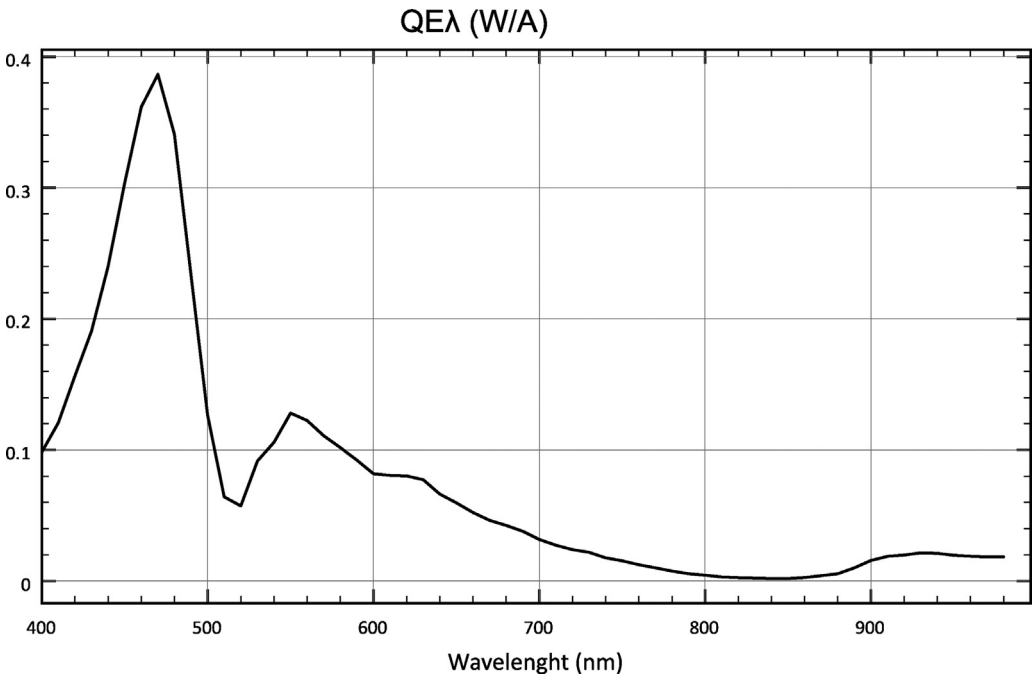


Fig. 21. Quantum efficiency plot of the p+/n–well photo diode. A = 1.44×10^{-6} cm^2.

photo diode is forward biased, the slope deduced from the trending line is greater (0.25) than when it is reversed biased (0.20). This indicates that in the first case a slightly higher V_{FG} value is reflected over the floating gate. This can be explained also from the coupling coefficient point of view. From Eq. (1) it can be seen that if the capacitance in the numerator is increased, the coupling coefficient will be increased in turn, although the total capacitance is affected too. If this is true, it can be deduced from (6) that V_{FG} will be increased also. Specifically, when the diode is forward biased, the junction depletion capacitance reaches a maximum and the resulting capacitance with C_{PH} in series has almost no variation. But on the contrary, when the junction is reversed biased, the junction depletion capacitance is reduced and the resultant capacitance with C_{PH} in series will result in a reduction, decreasing both the coupling coefficient and V_{FG}, as can be seen from the fitting equations shown in Fig. 15. This behavior is reversed if now the cathode is connected to the coupling capacitance, C_{PH}, as can be seen in Figs. 16 and 17. Again, the behaviors identified before can be seen when the photo diode is forward or reverse biased. Once again, from the trending line a slope of 0.25 was obtained when the photo diode is forward biased and 0.20 when in reverse bias. Then, from these results it is confirmed that a fraction of the voltage present at one terminal (anode or cathode) of the photo diode can be present over the floating gate. Besides, it is suggested that the behavior of V_{FG} is affected when this device is added between the biasing voltage source, V_{PH}, and the coupling capacitor C_{PH}, presenting in theory, different coupling coefficients depending on the way the photo diode is biased. Next, this fact is confirmed experimentally as shown in the following sections.

6. Experimental results

Several measurements were conducted, first for the LED used to illuminate the fabricated photo diode, and next for the photodiode. Encapsulated chips were used and initially, several chips were interconnected when the purpose was to measure two or three photo diodes in series, as will be explained next.

6.1. Optical characterization

In order to have the appropriate reference regarding the light source used to illuminate the p+/n–well photo structures, and to be able to correlate this data with the photo response of the fabricated structure, optical characterization was conducted and explained next.

6.1.1. Light source

The spectral response of an Ultrabright White LED device (VLHW5100) is shown in Fig. 18. Three different LEDs were tested and they show a high illumination peak around a wavelength of 450 nm, and two more peaks at 535 and 609 nm, respectively. It is important to remark the low level response of the LED at 650 nm, since as will be shown later, the fabricated photo structure has its higher photocurrent at this wavelength.

Also, the optical power delivered by the LED was measured and is shown in Fig. 19. It was characterized in a voltage range from 0 to 6 V applied to the LED.

Here it is also important to remark the behavior of the response of the LED as the applied voltage is increased, since this will be reflected when the photo diode is illuminated to obtained the I–V curves. As can be seen, the illumination power is rather linear from 2.6 V up to 4 V. However, if the LED is biased below 2.6 V, it does not light on and I–V curves for the photo sensor with the LED biased below this voltage will correspond to dark current. On the other side, when the LED is biased above 4 V, power begins to saturate, losing linearity.

6.1.2. p+/n–well photodiode

Next, the photo response of the p+/n–well structure described in Section 3 was measured using a monocromator Instruments SA, Inc., within a wavelength range of 400–970 nm. The results for photoconductivity and quantum efficiency are shown in Figs. 20 and 21, respectively. From the photocurrent response, a maximum is obtained in 650 nm and from the quantum efficiency response a maximum is obtained at around 450 nm. The experimental quantum efficiency obtained for this structure, fabricated with the C5 technology of On Semiconductor, is different from that obtained

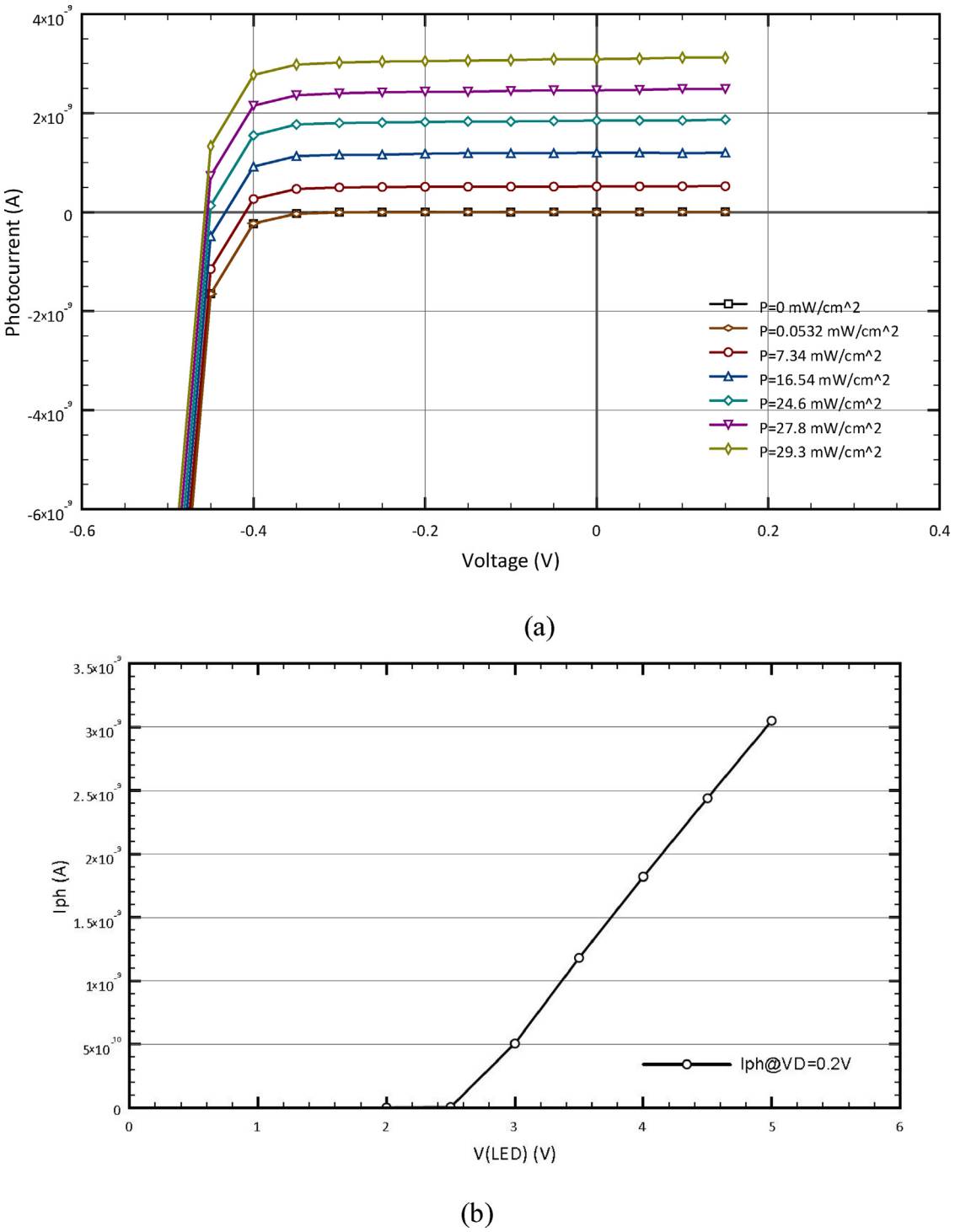
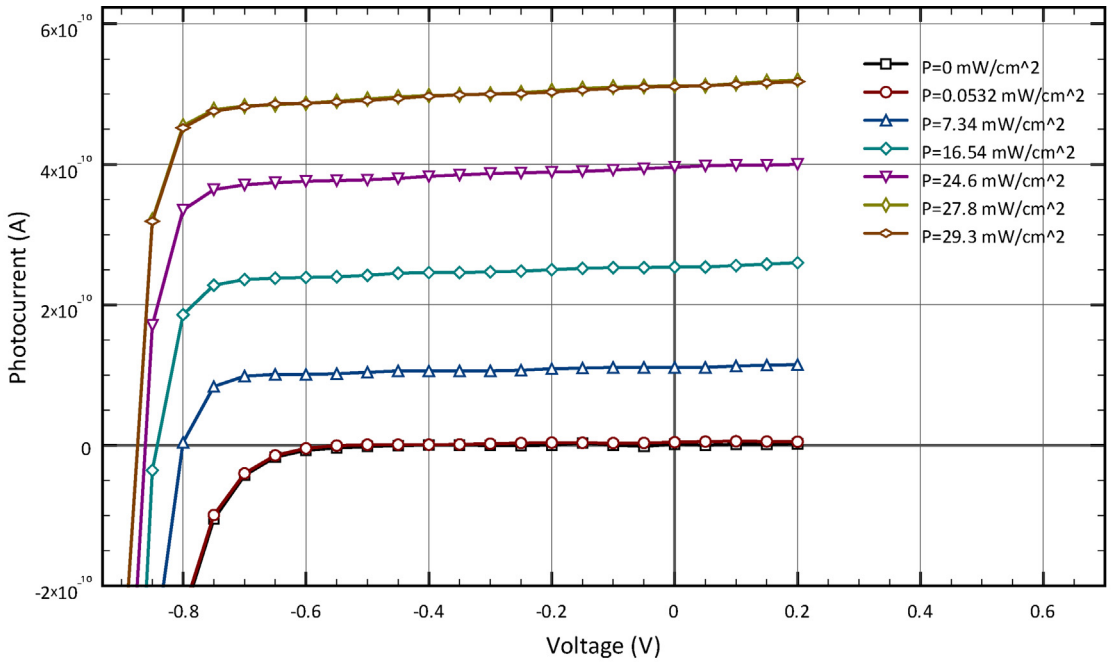


Fig. 22. a) I–V curve for a single photo diode after illuminating with different irradiance power; b) Photo current response of the photo diode as a function of voltage applied to the LED.

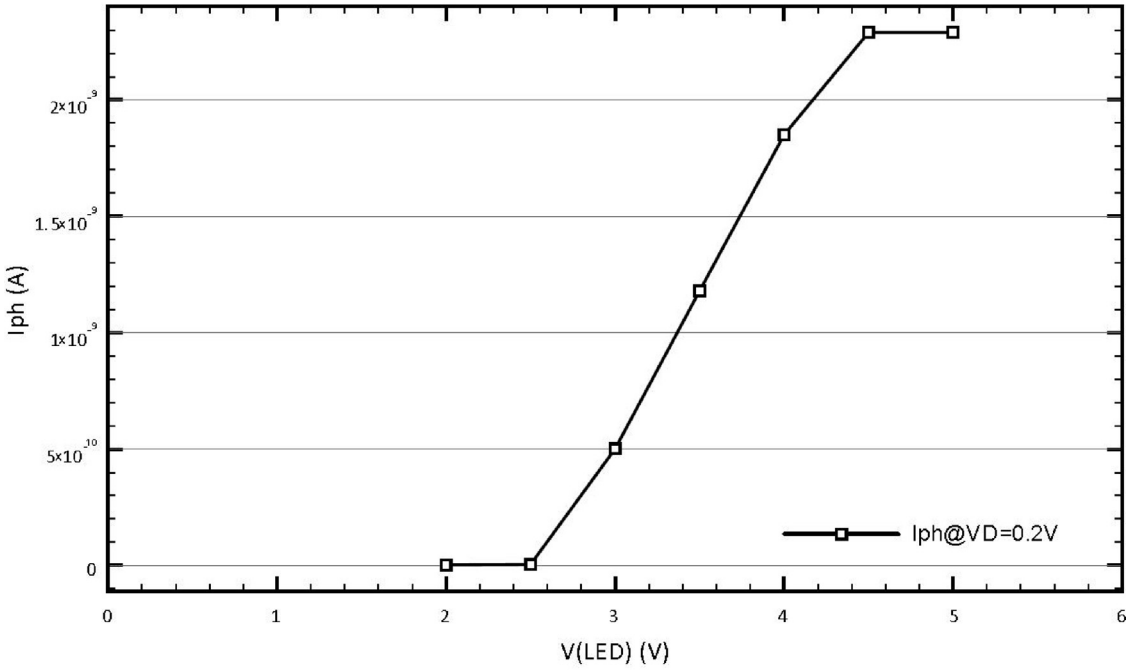
in [13], where the UMC 0.18 μm technology was used, it is important to remember that for the cell proposed in this paper, where the photo sensor will be connected to a control gate of a FGMOS, no photocurrent will flow and the only parameter of interest is the voltage at open–circuit, V_{OC}.

6.2. I–V curves of the fabricated photo sensor

Next, I–V curves were measured for the photo sensor not connected to the FGMOS, illuminating with the ultrabright white LED, mounted inside a black box where the chip was connected, as well. Different voltages were applied to the LED and the corresponding irradiance power is shown in Table 1, according to Fig. 19. It is well known that a series array of solar cells will result in an increase of V_{OC} depending on the number of photocells connected. Hence, three different results are shown next, where arrays correspond to a single photo diode, and two and three photo diodes connected in series. Here it is important to mention that the way the curves are presented is the result from the way the data was delivered by



(a)



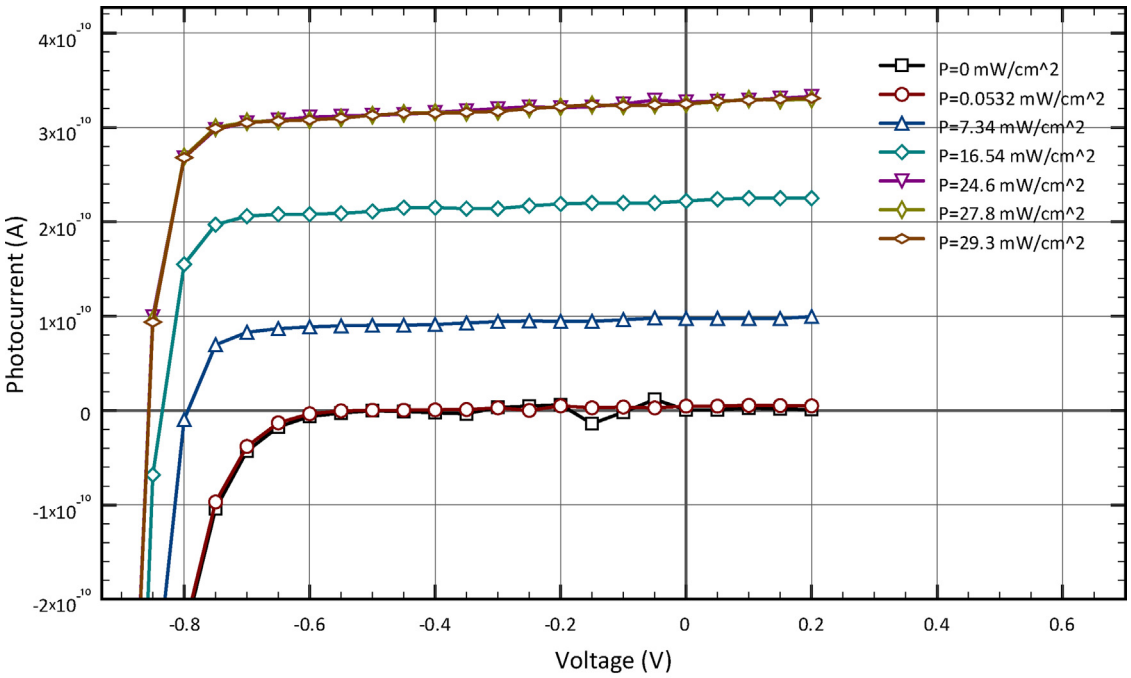
(b)

Fig. 23. a) I–V curve for two photo diodes connected in series after illuminating with different irradiance power; b) Photo current response of the photo diode as a function of voltage applied to the LED.

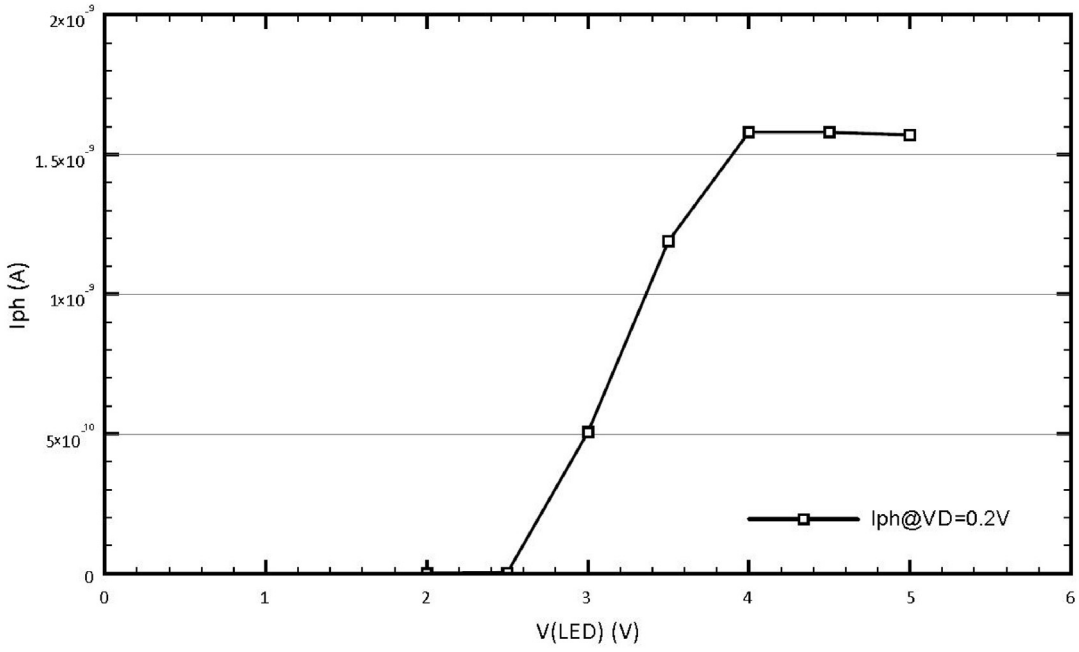
the Semiconductor Characterization System Model 4200 SCS, from Keithley, but they should be interpreted conventionally.

First, a single photo diode was measured, in dark and illumination and the I–V curves are shown in Fig. 22. It can be seen the regular increase in photo response for this photo diode and that V_{OC} is around −0.45 V. Curves in dark and when 2.5 V was applied to the LED are overlapping, according to the results shown in Fig. 17, indicating that 2.5 V is not yet enough to illuminate the photodiode, so only six curves can be identified. This behavior is present in all the following results.

Next, two photo diodes were interconnected in series, each one from separated encapsulated chips. The results are shown in Fig. 23. Here, it can be seen that V_{OC} was increased, due to the series array, to around −0.9 V. Note that the maximum current achieved with



(a)



(b)

Fig. 24. a) I–V curve for three photo diodes connected in series after illuminating with different irradiance power; b) Photo current response of the photo diode as a function of voltage applied to the LED.

an illuminating power of 29.3 mW/cm^2 is lower than with a single photo diode. This can be due to the increase in the series resistance of the array with two photo diodes of different chips, together with the fact that the response of the LED saturates beyond 25 mW/cm^2 as is shown in Fig. 19.

Here it should be noticed that although the inset considers seven illumination conditions, curves for 0, 0.0532, 27.8 and 29.3 mW/cm^2 are overlapped, due to response of the LED shown in Fig. 19, where saturation was found either at low or high applied voltages to the LED. Finally, three photo diodes from three different chips were connected in series and the result is shown in Fig. 24. Again, as expected, V_{OC} was increased to around −1.35 V, although it appears that the photocurrent cannot go further than 1.5 nA, since there is an increase in series resistance, decreasing the current that can flow through the series array, compared with the current through a single photo diode or a series array of two photo

Table 1
Corresponding irradiance power with voltage applied to the ultrabright white LED.

Voltage across the LED (V)	Irradiance power (mW/cm^2)
<2.6	0
2.5	0.0532
3.0	7.34
3.5	16.54
4.0	24.6
4.5	27.8
5.0	29.3

diodes. Also, here it is evident that the non–linearity of the LED's illumination is the responsible that only four from seven illumination conditions for the photo diode are shown, where overlapping is present also at low and high applied voltages to the LED.

Then, after these measurements, it is clear that depending on the number of photo diodes connected in series, different modulation voltages can be present upon the control gate of a FGMOS and this can be used as well, to affect the I–V response of the FGMOS. It is convenient to remember that the purpose of this work is to demonstrate that this V_{OC} can be capacitively coupled to the floating gate of the FGMOS, with the anode or the cathode of the photo sensor being one of the plates of the coupling capacitor. Moreover, a single FGMOS can have more than one control gate where each one can be driven by a photo diode (or photo diodes array). It would be interesting to test the operating principle proposed with these different options as an active pixel, where only one transistor may be used to perform the image processing.

6.3. I–V response of the photo diodes connected to the FGMOS

Structures shown in Fig. 7 were measured in dark and with light using an illumination of 29.3 mW/cm^2 and the results are shown next. The first measured structure corresponds to the configuration shown in Fig. 8, where the anode is connected to the coupling capacitor having an area A = 20.4 μmx20.4 μm. A voltage sweep was applied to the terminal label *VCG* and three different voltages were applied to V_{PH}: 0 V, 1.8 V and −1.8 V, both in dark and illumination. The magnitude of ±1.8 V applied to V_{PH} is to assure that the diode will be reversed biased when connected to the anode or cathode. As it is well known, when the diode is forward biased, the associated p–n junction depletion capacitance is large, and when reverse biased, it is small. This will influence the I–V characteristics of the photo diode–FGMOS configuration, as will be shown next. Fig. 25(a) shows the transconductance plot when measured in dark and Fig. 25(b) in illumination.

As the simulation in Fig. 15 shows, when a negative voltage is applied to V_{PH} the coupling coefficient is bigger than when a positive voltage is applied. This is more evident when the structure is illuminated, confirming the behavior anticipated with simulation. Also, it can be mentioned that this measurement demonstrates that the voltage applied to V_{PH} is effectively coupled to the floating gate of the FGMOS transistor via the coupling capacitor, but also that illumination can influence the I–V characteristics of a FGMOS transistor, as well. Next, Fig. 26 shows the results obtained after measuring the configuration shown in Fig. 9, where this time V_{PH} is applied to the anode of the photo diode.

From these figures, it should be noted that the transconductance response even in dark and in illumination, present an offset current and a different response compared to that obtained when V_{PH} drives the cathode, as in Fig. 25, specifically when the photo diode is forward biased, i.e. when 1.8 V is applied to V_{PH}. This may be explained considering that in this situation V_{PH} could be present across the parasitic diode formed with the layers p+/N–well/p–substrate/N–well along the structure photo diode–p–MOS transistor. Since the bulk of the p–MOS transistor (N–well) is short–circuited to the transistor's source, this may establish a conduction condition for the transistor that could be responsible for that offset. However, even though the non–expected response, once more it is shown that the voltage can be coupled through the photo diode and the coupling capacitor. Moreover, light has not the same effect seen in Fig. 25, where current through the FGMOS was increased when illuminated. This deviation from the expected response may be due to the kind of structure selected, this is, it will be interesting to prove a similar configuration but with n–FGMOS transistors instead of p–FGMOS, to see if this behavior is not present. Also, the transconductance curves when V_{PH} = 0 V and V_{PH} = −1.8 V overlap each other, making no difference between the photo diode response in equilibrium and reverse biased. Hence, there is no advantage applying either higher forward voltages or illumination.

Now, a similar configuration like that shown in Fig. 8 but with a coupling capacitor with twice the area A (see Fig. 7(c)) was measured and as Fig. 27 shows, the results are similar to those shown in Fig. 25.

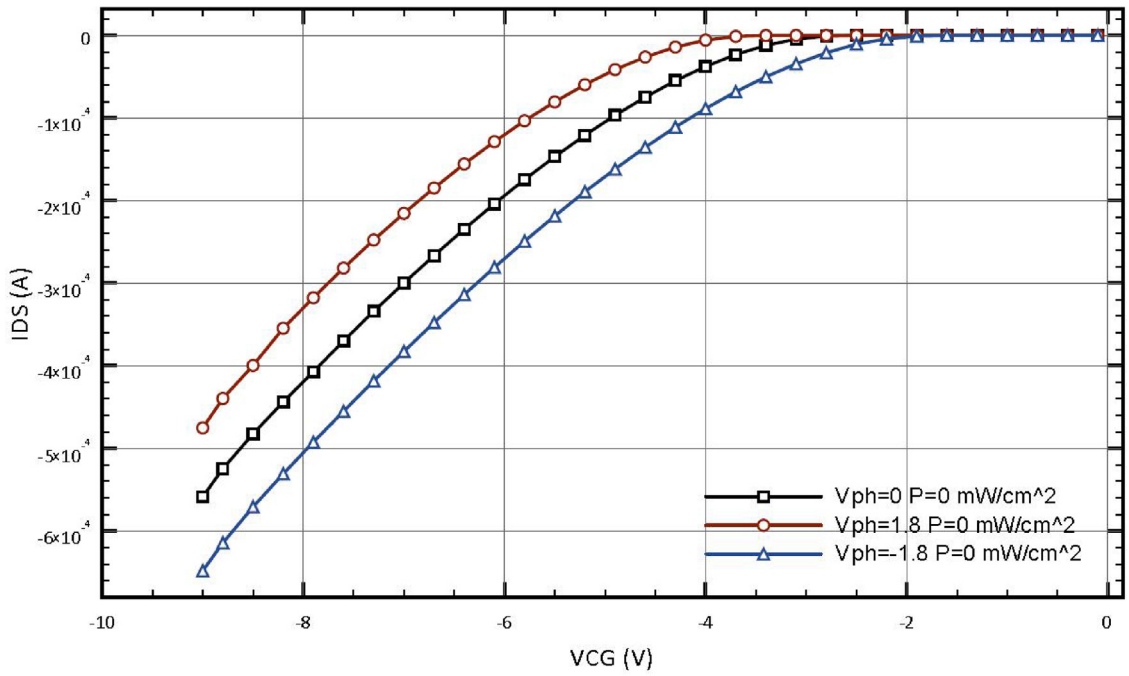
It can be seen also that due to a larger area in the coupling capacitor used in this configuration, the expected behavior resulting in different coupling coefficients when forward or reverse biased, is more evident than in Fig. 25. This suggests that a trade–off must be considered between the areas of the structure and the configuration of a desired system, such that a large integration can be made for a specific function. Also, from this last result it seems to be clear that for this structure (N–well cathode–p+ anode–coupling capacitor–FGMOS), better and reliable results are obtained when an external voltage (V_{PH} in this case) is applied to the cathode of the photo diode, rather than to the anode.

Now, a configuration like that shown in Fig. 9, but with a coupling capacitor with twice the area A was measured and the results in dark and illumination are shown in Fig. 28. As it can be seen, these are very similar to those shown in Fig. 26, indicating once more that using this structure with the anode connected to V_{PH} gives results different from those obtained with simulation.

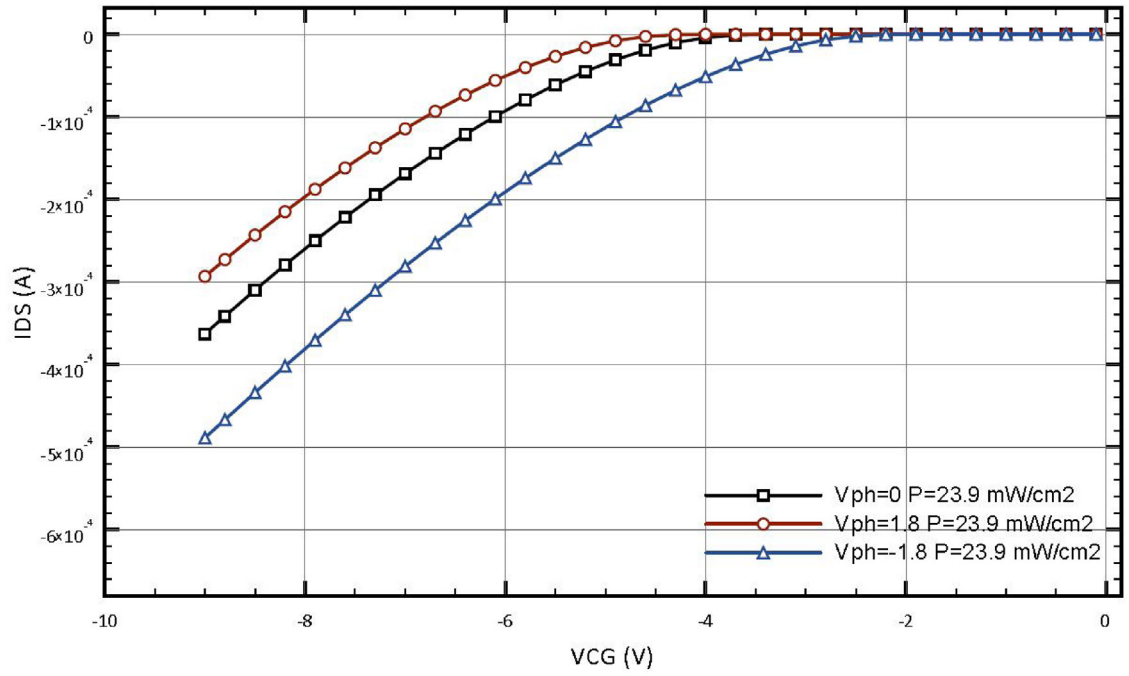
Now, the next structure measured was the one shown in Fig. 10 and the results are shown in Fig. 29, where three photo diodes in series are connected to the coupling capacitor with Area = 6A and V_{PH} driving the anode of the photo diode. Here, it should be noticed that the transconductance curve is shifted to the left due to the sum of the open–circuit voltage, V_{OC}, of each photo diode. Although this structure presents an irregular behavior regarding what could be expected, it can be mentioned that together with an effective voltage coupling to the floating gate, this voltage can be modulated with a series array of photo diodes when they are illuminated. However, an offset current is present, as was obtained too in the measurements presented in Fig. 28, giving indication that it is not so convenient to connect V_{PH} to the anode using this structure.

Finally, the structure shown in Fig. 11, was measured. This configuration has three photo diodes in parallel, each with a coupling capacitor with an Area = 2A and V_{PH} connected to the three anodes at the same time. The results are plotted in Fig. 30.

The effects that can be mentioned for this configuration are the following. Due to the parallel array of the photo diodes, the depletion capacitances are added, increasing in consequence the magnitude of the coupling capacitance, thus the coupling coefficient. This helps to have a bigger fraction of V_{PH} over the floating gate, V_{FG}, which can drive more current along the FGMOS, compared to the configuration with a series array of photo diodes. On the other side, it can be seen that there is no adding of V_{OC} of each photo diode since they are in parallel. Here it should be remembered that there is no current flow through the transistor's gate, so the typical short–circuit current, I_{SC}, must not be taken into account.



(a)

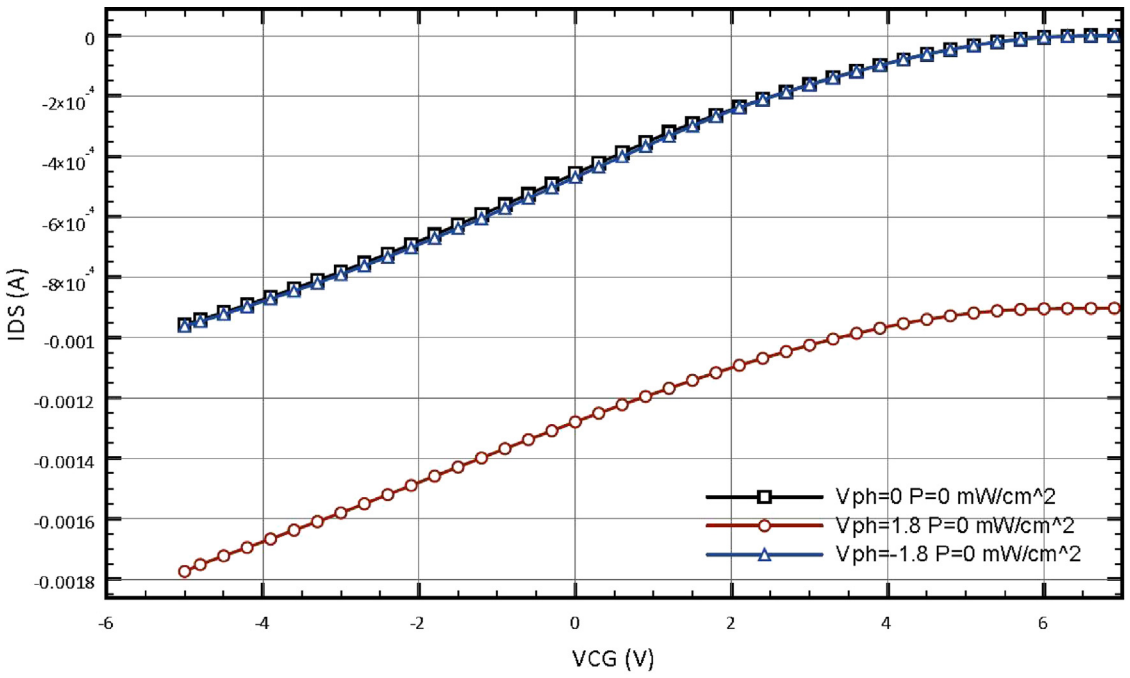


(b)

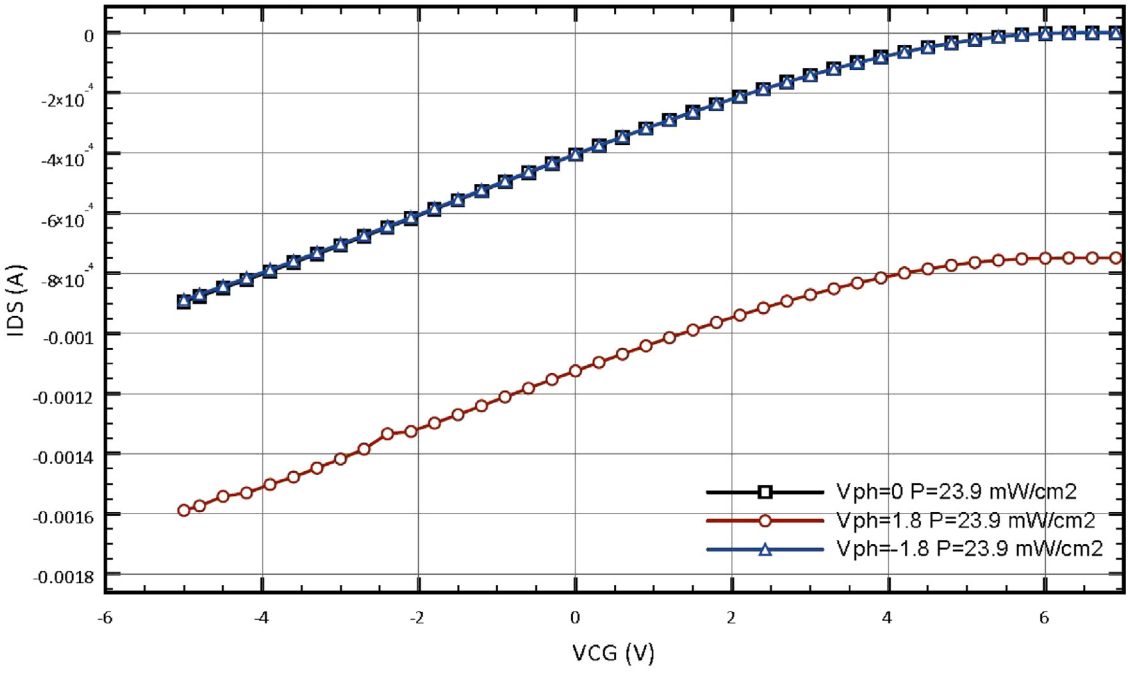
Fig. 25. Transconductance plot for the configuration of Fig. 5; a) in dark: b) with illumination.

7. Discussion

The hypothesis established at the beginning of this paper was that the typical open–circuit voltage of a micro photo cell can be able to modulate the I–V characteristics of a FGMOS transistor if it could be coupled to the floating gate via a coupling capacitor. The purpose of this work is to demonstrate two facts, i.e., that a photo diode can be used as a control gate when designing a FGMOS, and that when illuminating an array of photo diodes, the threshold voltage of these devices can be modulated. After all the measurements made using different configurations and orientations of the photo diode connected to a coupling capacitor, it was shown that it is possible to have a fraction of the voltage applied to one terminal of the photo diode even in dark conditions, and furthermore, when it is illuminated the fraction of the corresponding open–circuit voltage, V_{OC}, is present on the floating gate that can still modulate the I–V characteristics of the FGMOS transistor. However, better results close to those obtained previously by sim-



(a)



(b)

Fig. 26. Transconductance plot for the configuration of Fig. 6; a) in dark: b) with illumination.

ulation, were obtained when the cathode of the photo diode was connected to the applied voltage. Here it is speculated that the reason for the non expected response when the excitation was feed through the anode, is because of the construction of the structure, where the cathode is made with the N–well and the bulk of the MOS transistor is also a N–well short–circuited with the source, introducing a parasitic series diode array that may create a direct path for the bias applied to the photo diode creating a conduction condition to the FGMOS transistor. This gives the idea to make different designs using a N–FGMOS transistor, for instance. This extra study can include different coupling capacitors areas for control gates, different metallization patterns for the illuminated area of the micro photo cell, etc. This work can be directed to use these kinds of structures as an active pixel since one transistor can receive the information of several photo sensors, reducing the complexity of actual pixel designs.

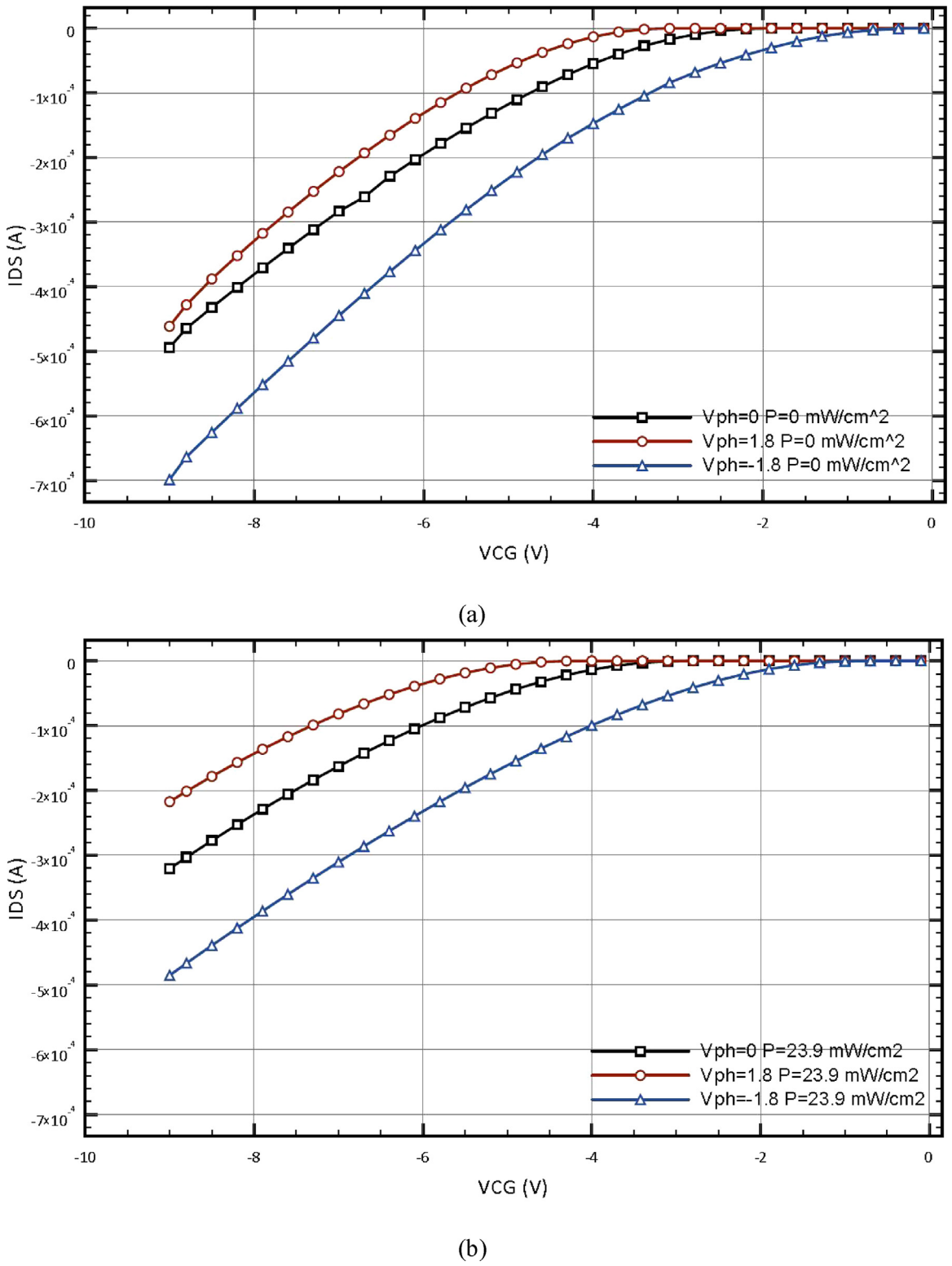


Fig. 27. Transconductance plot for the configuration of Fig. 5 with a coupling capacitor with Area = 2A; a) in dark: b) with illumination.

8. Conclusions

First of all, it is necessary to precise that the native threshold voltage of "the inner or embedded" MOSFET" used in the FGMOS keeps unaltered all the time independently if the FGMOS operates as a non-volatile or a volatile device and it should be noticed that the measured threshold voltage considering a FGMOS is called "apparent threshold voltage" since it is obtained as a function of the applied voltage over the control gate, V_{CG}, not as a function of the voltage present on the floating gate, V_{FG}, since it is fixed once it is programmed. It should be remembered that plots for apparent threshold voltage extrapolation, $V_{TH}{}^{*}$, are made when a sweep voltage is applied to the control gate, V_{CG}. To understand the notation, specifically, V_{TH} is the native threshold voltage of

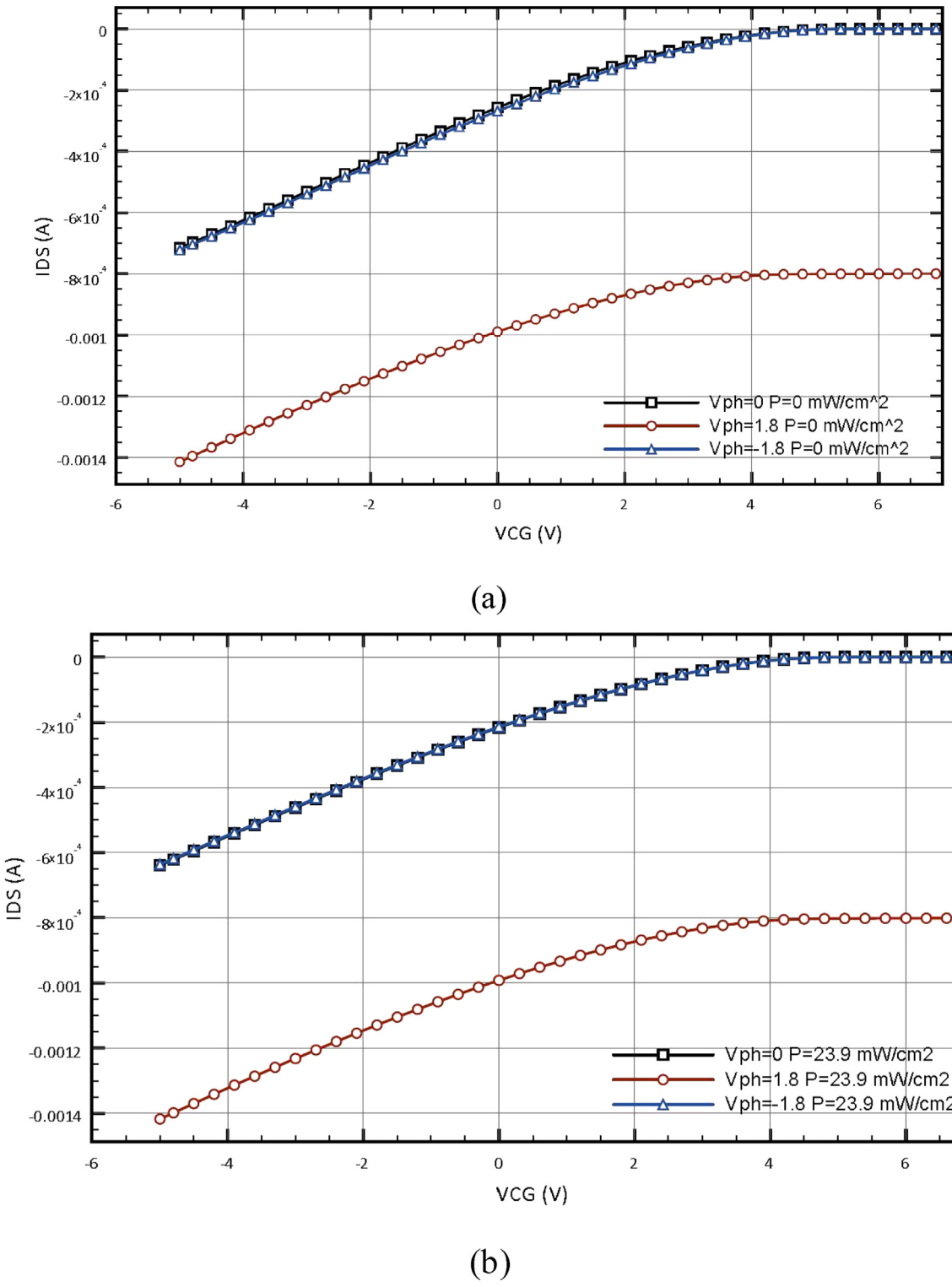
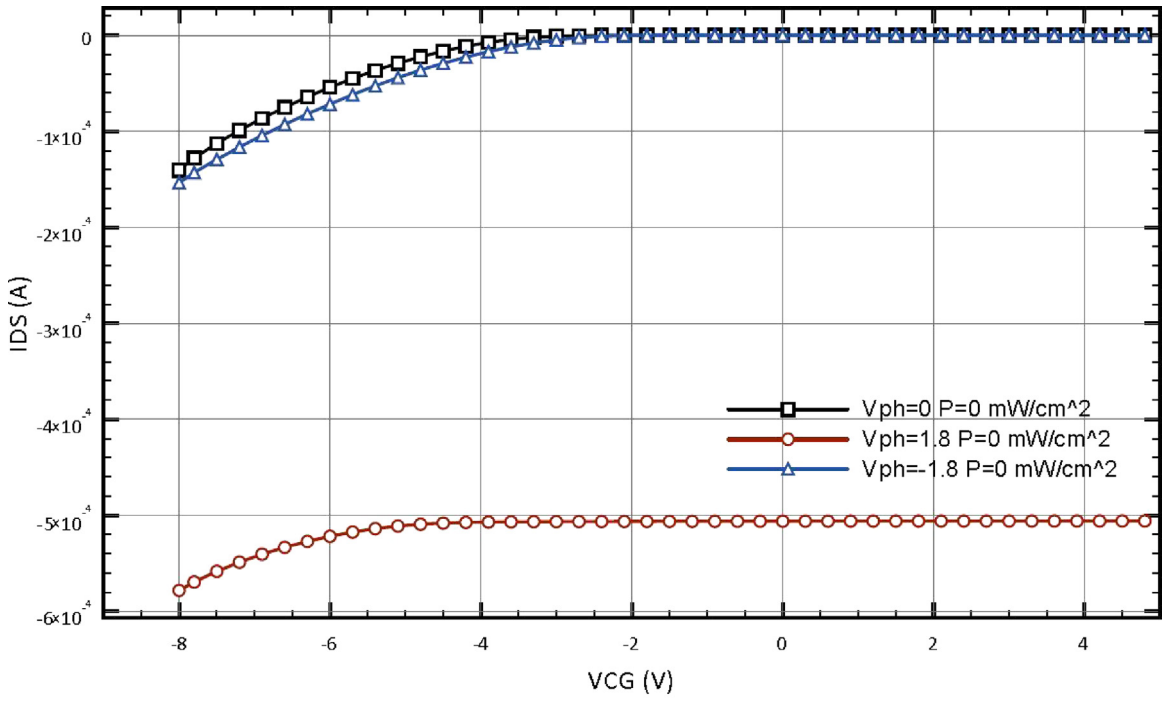
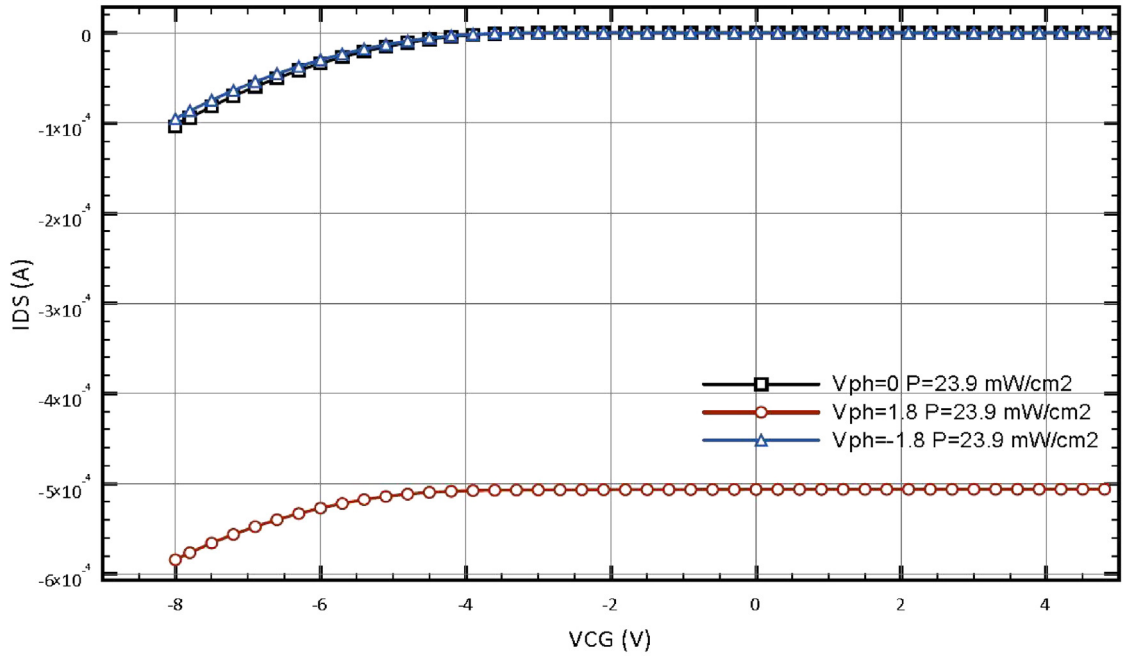


Fig. 28. Transconductance plot for the configuration of Fig. 6 with a coupling capacitor with Area = 2A; a) in dark: b) with illumination.

the embedded MOSFET, and V_{TH}^* is the apparent threshold voltage of the FGMOS, and the later can be modulated having at last either a volatile or non-volatile FGMOS. It is well known that FGMOS transistors can be operated as a non-volatile memory when charge is injected/extracted to/from the floating gate keeping this condition meanwhile this charge is not removed by known injection/extraction methods like Fowler-Nordheim or Hot Electrons. Besides, FGMOS can be operated also as a volatile device when only an external voltage is applied to the control gate(s) and coupled to the floating gate, this is, when no injection/extraction of charge is promoted by electrical means, modulating anyway the I–V characteristics, as well, as long as the voltage is being applied to the control gate. Once this control gate voltage is removed, the FGMOS will return to its original condition. But also it should be remarked that in neither case the native threshold voltage is modified at all. For the case reported in the paper, it is shown by simulation and



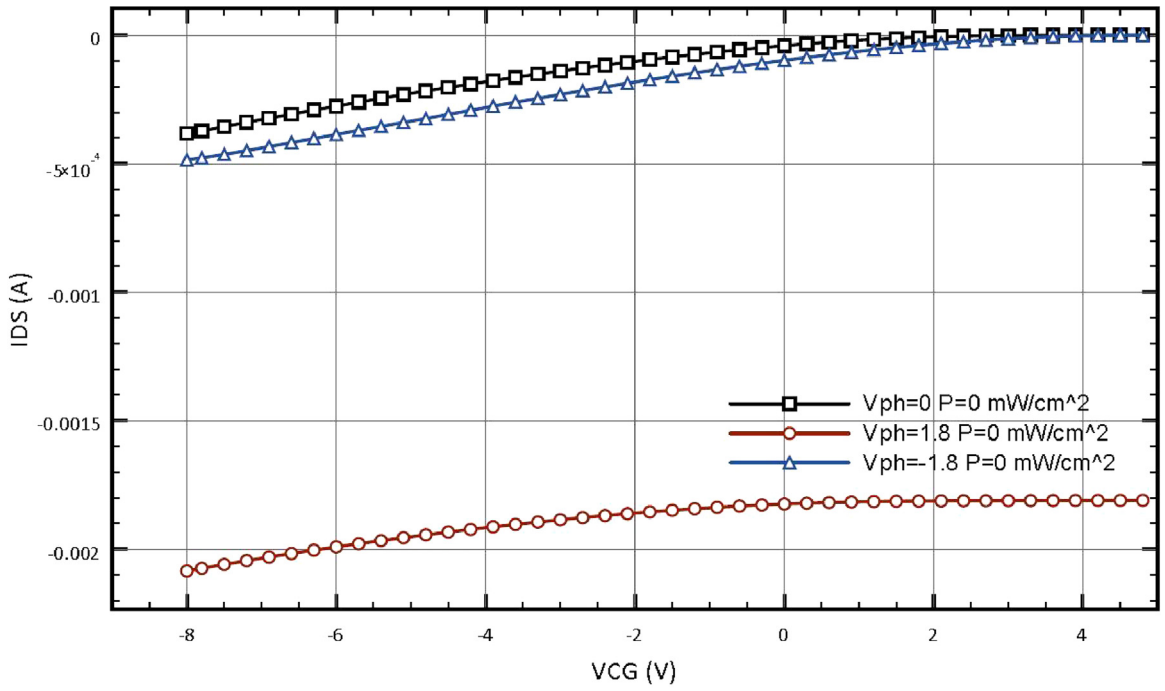
(a)



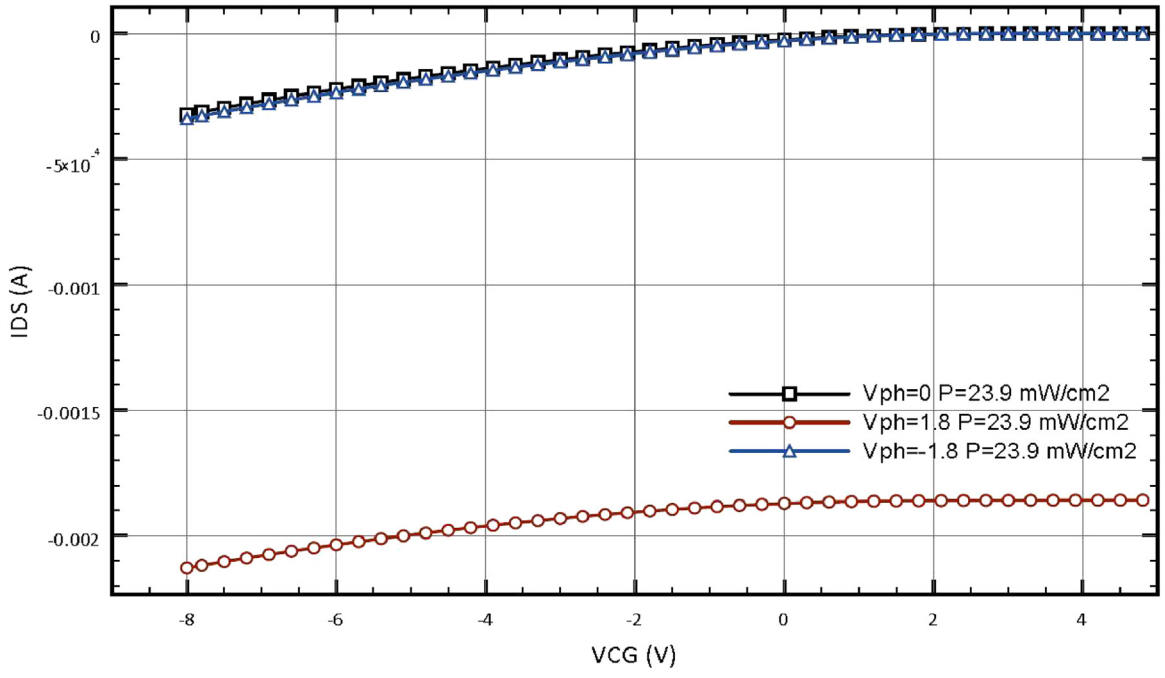
(b)

Fig. 29. Transconductance plot for the configuration of Fig. 7 with three photo diodes in series and a coupling capacitor with Area = 6A; a) in dark: b) with illumination.

experimentally, that using the FGMOS operating as a voltammetric sensor, the open circuit voltage, V_{OC}, of a micro photo diode, can be coupled to the floating gate using the anode or cathode of this photo diode as the control gate, from which the FGMOS in this proposal will operate as a volatile device since no charge is involved in the modulation of the I–V characteristics. Also it is well known that the junction capacitance of a diode can be modulated depending on if the junction is forward or reverse biased. This introduces a voltage dependent variable coupling capacitance that will in consequence influence the value that will be present over the floating gate, as can be deduced from Eq. (11).



(a)



(b)

Fig. 30. Transconductance plot for the configuration of Fig. 8 with three photo diodes in parallel and a coupling capacitor with Area = 2A for each photo diode; a) in dark: b) with illumination.

With this work, it was demonstrated that it is possible to use a photo diode as a control gate and to modulate the I–V characteristics of a FGMOS transistor in dark and with illumination, something that until now is not reported yet. This can be achieved since a fraction of the input voltage can be present over the floating gate via a coupling capacitor with no necessity of voltage integration with the parasitic capacitance of the transistor, as is done with conventional pixel configurations. Moreover, this was possible either in dark or illumination, with better results when the exciting voltage was connected to the cathode of the photo diode, with the structure

constructed in this work. Also, when illuminated and depending on the photo diode array used, it was possible to modulate the I–V characteristics of the FGMOS with the typical open–circuit voltage, V_{OC}, of a photo sensor, this is, with a series array of a certain number of photo diodes. Hence, a demonstration is done that it can be induced also a voltage upon the floating gate coming from an optical phenomenon different to the conventional Hot Electron Injection or Fowler–Nordheim tunneling. This study can be extended further to examine the possible application of this structure in active pixels.

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