



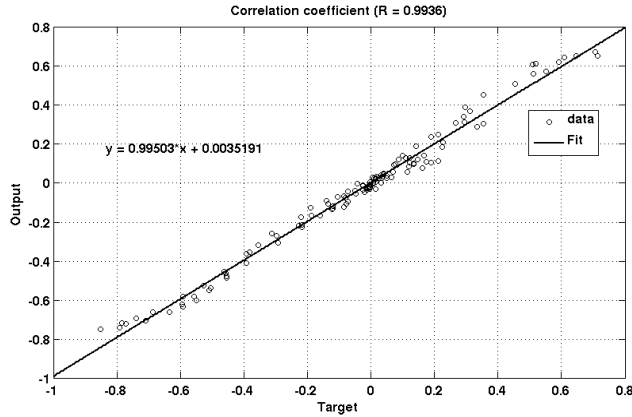








In Fig. 11 is presented a scatter plot with the regression line and the line equation that will help us to make future predictions about the output that would produce our digital system from any input value. Additionally, it is shown the Pearson correlation coefficient, which indicates the degree of dependence between expected test data and the output data of the digital system and it has a value  $R = 0.9936$ .



**Fig. 11** Correlation coefficient (R) for the test set and 2-5-2-1 architecture.

The results can not to be compared directly with other previous studies, as each study takes a different focus, using different architectures and implemented in different technologies. However, we can mention that in this work focused on the optimization of resources (one DSP by neuron) and train the network using a protocol type batch. Table 3 compares these features with other studies.

## V. CONCLUSIONS

In this paper, we presented the implementation of an ANN architecture with Back Propagation training algorithm. It is reconfigurable, allowing us to change its learning rate and training epochs in hardware to train the network in real time without the need of reprogramming the FPGA for each change of these parameters.

Serial processing implementation allows significant saving of FPGA logical resources, but the main drawback of this technique is in reducing its performance, increasing the network response time, which was 1.96 ms per epoch for a 50 MHz clock signal. In this first version the number of training epochs was implemented as stopping criterion; for

an improved version we want to add more stop criteria to achieve a better performance of the training algorithm. Another point to consider is to include a routine for generating random initial weights and biases within the implemented system.

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**Table 3.** Performance comparison

Reference	Architecture	Precision	MSE	Protocol	Focus	DSP's
This work	2-5-2-1	16-bit fixed-point	0.00143	Batch	Serie	11
[5]	5-3-3	16-bit fixed-point	0.03	stochastic	Parallel	--
[4]	2-6-3-2	16-bit fixed-point	0.05	On-line	Pipelined	--
[6]	1-2-1	18-bit fixed-point	--	On-line	Pipelined	14