

Design of a CMOS-based RF-MEMS Switch as an Alternative Charge/Discharge Mechanism for quasi Floating-Gate MOS Transistors

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Abstract – In this paper a quasi-floating-gate charge/discharge method is presented and a novel application for the widely used membrane-like RF-MEMS switches is proposed as well. The design of a four-beam capacitive MEMS structure is described within the 0.5 microns (2P3M) CMOS technology framework. Furthermore, the device is electromechanically simulated in the COMSOL Multiphysics suite and electrically simulated via a custom SPICE model. Finally, the possible use as an electromechanical switch to provide an initial desired electric potential to the floating gate in a floating-gate MOS transistor (FGMOS) device is discussed.

Keywords – RF-MEMS, quasi floating-gate, capacitive actuation, capacitive MEMS, FGMOS, COMSOL.

I. INTRODUCTION

Commonly used in the Micro-Electro-Mechanical Systems (MEMS) technology, the capacitive contact and shunt switches have always been an effective actuation element for those systems needing a tunable filtering and dynamic high isolation mechanisms for RF signals. Besides the radiofrequency applications and devices, one of the most common issues in floating-gate CMOS applications are those associated in which non-desired floating electric charge and its related threshold voltage shift, are also involved. Since both floating-gate MOSFETs and MEMS micro-actuators are suitable for being developed in standard CMOS processes, a membrane-like MEMS micro-actuator design is implemented heading to a dynamic electro-mechanical access to the floating potential terminal, so a desired offset potential can be set and sustained for the benefit of the previously defined and expected operation of the involved floating-gate devices.

Since fixed-fixed beam structures has been proven to be more sensitive to the Joule heating effects [1], the architecture used in this work is the four-beam version shown in fig.1. This structure has anchors in the four beam tips and a squared membrane (120 microns per side, with four springs 126 μ m long) suspended in the middle. The membrane, designed to be fabricated in the Metal 3 (TiN/AlCu/TiN) layer of the OnSemi C5 [2] CMOS technology, is intended to be pulled down by

electrostatic force and make contact with the gapped Metal 2 transmission line below. Even though the pull-in voltage is desirable to be the lowest and the separation gap between plates in a capacitive actuator is directly related, the Poly 1 layer (polycrystalline silicon) was selected to be the trigger terminal due to non-convergent simulation issues with COMSOL in the vicinity of the pull-in voltage. So, according to the equivalent circuit shown in Fig. 2, the membrane shall move downwards when a significant potential difference (in the order of 10 volts for this proposal) appears between the poly 1 plate and the membrane itself.

II. THEORETICAL APPROACHES

The membrane/beams system can be reinterpreted as a mass-spring dynamical system (as shown in Fig.3) in which the membrane is pulled down by an electrostatic force, F_e , against the restoring spring force, F_k , due to the beams flexion. Since the electric attractive force has its source in the applied voltage and the restoring force is proportional to an equivalent elastic constant k , there is a pull-in point in which the latter is weaker and the contact with the plate below is imminent. In this point, the applied voltage is denoted as the pull-in voltage V_p .

$$F = F_e + F_k = \frac{1}{2} \frac{\epsilon A}{(d-x)^2} V^2 - kx \quad (1)$$

$$V_p = \sqrt{\frac{4}{27} \sqrt{\frac{2kd^3}{\epsilon A}}} \quad (2)$$

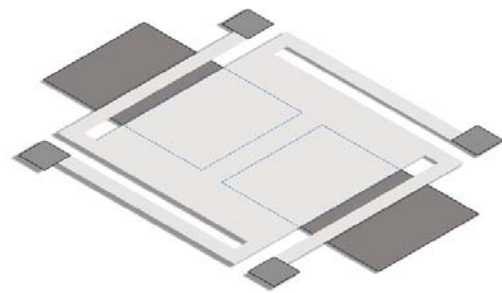


Fig. 1. Four-beam membrane-like capacitive structure.

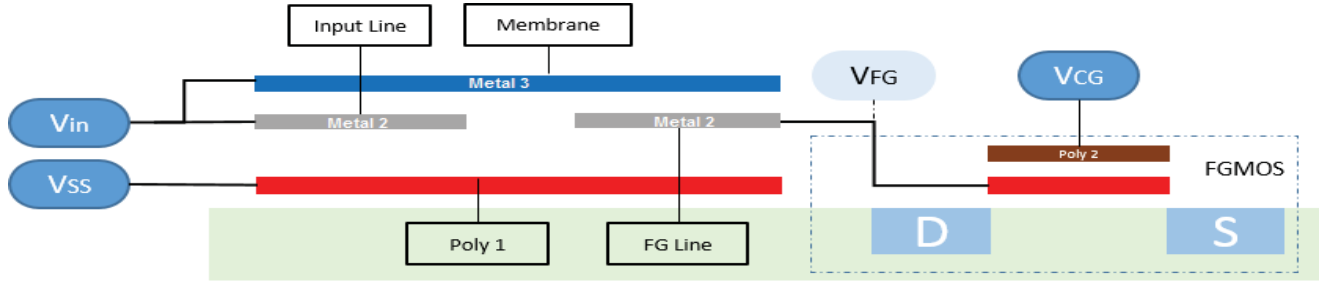


Fig. 2. MEMS-FGMOS equivalent circuit.

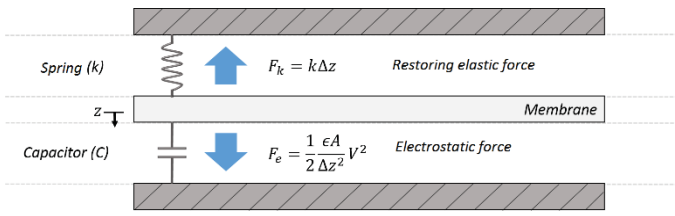


Fig. 3. Equivalent mass-spring system.

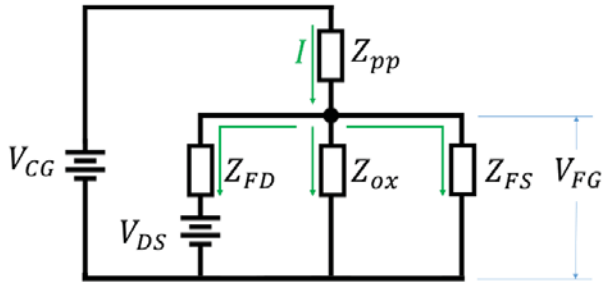


Fig. 4. Impedances in the FGMOS simplified model.

By the way, the pull-in voltage is proven to be reached at a displacement of 1/3 of the original gap [3], which in this case, is slightly greater than the separation between the Metal 3 membrane and the Metal 2 transmission line so the further pull-in voltage effects are negligible in the described device.

On the other hand, the floating-gate MOSFET analysis is focused in the potentials of each one of its terminals. The equivalent circuit in Fig. 4 represents the Poly 2 to Poly 1, Poly 1 to substrate (gate oxide), and gate-substrate parasitic capacitors as impedance elements. Although the charge/discharge membrane mechanism described is a quasi-floating-gate approach due to the inclusion of an external switching system, electrically, the FGMOS transistor designed for this application can be modeled as a fully floating-gate device as long as the MEMS switch is open ($R_{off} \rightarrow \infty$). For a capacitive coupling coefficient $K_{CG} = C_{pp}/C_{TOT}^*$, $C_{TOT}^* = C_{FS} + C_{ox} + C_{FD} + C_{pp}$, and a factor $f = C_{FD}/C_{pp}$, the coupled potential in the floating gate is given by:

$$V_{FG} = K_{CG}(V_{CG} + fV_{DS}) \quad (3)$$

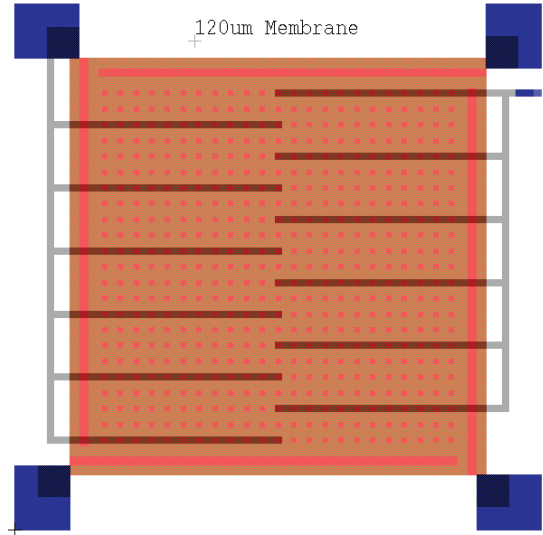


Fig. 5. Integrated circuit CAD membrane design including the Poly 1 layer.

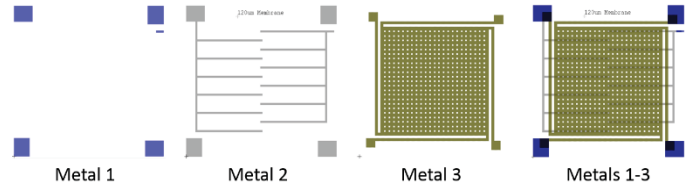


Fig. 6. Integrated circuit CAD metals sequence.

that modulates the threshold voltage of the associated MOSFET as a function of the controlling-gate potential V_{CG} and the drain to source voltage V_{DS} .

Therefore, the concern is to model and evaluate the performance of the proposed structure based in a standard CMOS technology in order to extend its application either as a floating-gate discharge option, or to operate the FGMOS within the quasi-floating regime.

III. METHODS AND SIMULATIONS

For the topologic design of integrated circuits the L-Edit suite from Tanner is used. In this example a 120-micron square membrane shown in figure 5 is drawn via the CAD software

following the sequence from figure 6 and adding a Poly 1 layer underneath. The N and P floating-gate transistors shown in figure 7 were also drawn and their capacitive parameters extracted as a reference for SPICE simulation. The dimensions in the test transistors are $L = 3\mu\text{m}$ (10λ), $W = 9\mu\text{m}$ (30λ) for the N-type MOSFET and $L = 3\mu\text{m}$ (10λ), $W = 27\mu\text{m}$ (90λ) for the P-type MOSFET.

Once the structure was defined, the electromechanical simulation in the COMSOL Multiphysics platform started with the geometrical definitions of the solid bodies representing each one of the CMOS technology layers involved. Besides the Metal 3 Membrane (figure 8-a), the multiphysics model includes the air gap, the Metal 2 transmission line, the SiO₂ bulk and the Poly 1 trigger sheet domains as well. Looking for the minimum interference of the transmission line to the electrostatic field between the Poly 1 plate and the membrane, Input and Floating Gate lines using the Metal 2 layer, are drawn in a narrow comb-like array, as seen in figure 8-b. For this set of domains, a pure mechanical characterization, a Joule heating related and the main electromechanical simulations were performed. In the mechanical characterization a $1\mu\text{N}$ test load force pushes the membrane down looking for the force-displacement ratio (elastic constant k) and the main stresses on the membrane surface. For the Joule heating simulation a $1\text{mV} - 5\text{mV}$ voltage drop range was applied over the membrane surface having two opposite (mechanically constrained) beam tips as terminals and looking for the maximum thermal expansion deformations. On the other hand, for the electromechanical simulation an electric potential difference (0 to 10V) was applied between the Poly 1 and Metal 3 plates configuring and attractive electrostatic force hence reducing the gap in the middle.

Finally, the circuit and SPICE models shown in figure 9 were tested using the biasing scheme presented by Kotani et al [4], also implemented by Ponce-Ponce [5] and Molinar-Solis [6] as a pulse-controlled quasi floating-gate charging method based on the FGMOS structure and properties analysis by Ramirez-Angulo et al. [7][8][9].

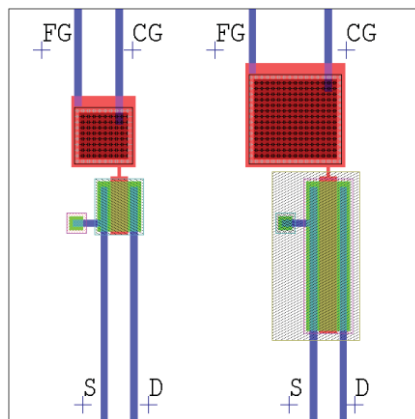


Fig. 7. Reference FGMOS transistors

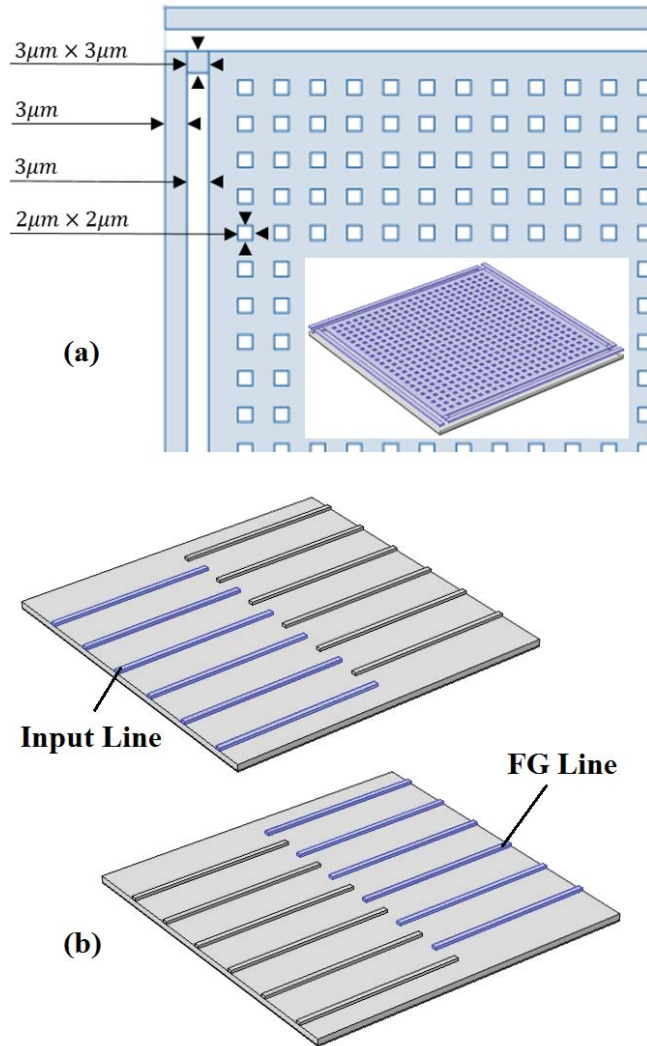


Fig. 8. $120\mu\text{m}$ membrane COMSOL Multiphysics domain.

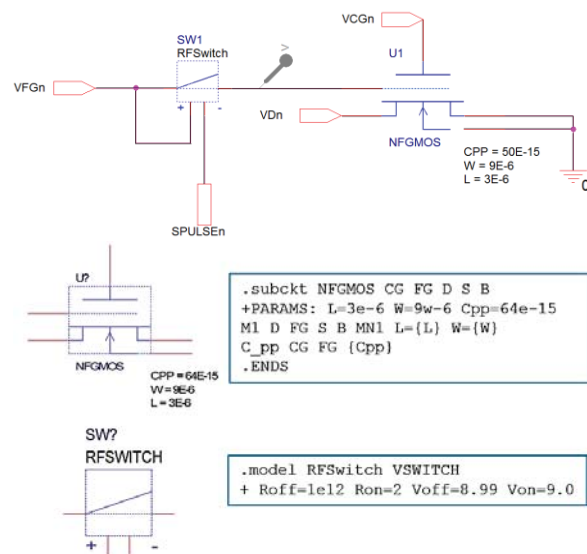


Fig. 9. SPICE circuit and model implementations.

IV. RESULTS

From the mechanical characterization, an equivalent elastic constant $k = 0.9$ resulted as the combined effect of the four $126\mu\text{m}$ beams, is present, and the maximum stress (43.5MPa) illustrated in figure 10 takes place in the beam-membrane joint. This amount of stress does not reach the plastic deformation stress which is reported [10] to be over 70MPa for most aluminum compounds.

On the other side, the Joule heating reveals a maximum thermal expansion displacement (fig. 11) of $0.11\mu\text{m}$ in the beam-membrane joint which is negligible for a 120-micron beam. This maximum displacement is reached at a 5mV voltage drop which is quite high for a low resistive body such as an aluminum alloy membrane. The study also shows a safe temperature rising (fig. 12) from room temperature to about 60°C in the same 5mV range.

Next, in the electromechanical analysis, figure 13 shows the displacement of a membrane being pulled down by an electrostatic force as a function of the applied voltage and the square membrane's side length. For an initial air gap of $1\mu\text{m}$ between the membrane and the transmission line, the 120, 130, 140 and 150-microns (and so on) membranes reach the total displacement with potentials under 10V, which is due to the beams' stiffness loss as the membrane size increases.

For the simulation, the effect of a floating potential on the displacement was also considered. Providing the transmission line (FG terminal) with a test potential of $-1, 0$ and 1V , the displacement for a $120\mu\text{m}$ membrane is affected (fig. 14) as a result of the superposition of attractive forces.

The SPICE electrical simulation confirms the expected system performance as the floating potential can be set throughout the RF switch and sustained by the floating-gate MOSFET conventional terminals using a non-overlapping voltage pulse mechanism (fig. 15).

The transconductance characteristic shown in fig. 16 shows the shift of the I-V curves of the FGMOS as a result of different test floating-gate potentials previously charged via the RF switch, as it was expected.

This simulation profile includes a test refresh signal period of 1ms (1kHz) which is not related to any natural resonance frequency but, it is important to notice that the main purpose of the system is to sustain a quasi-floating voltage in the floating-gate terminal which is a dc application.

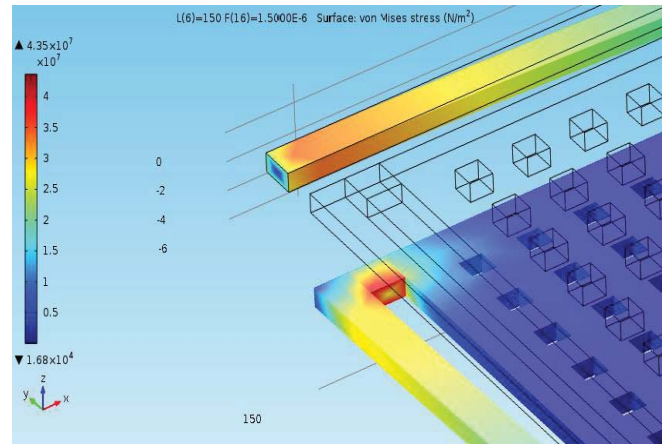


Fig. 10. Mechanical stress (MPa).

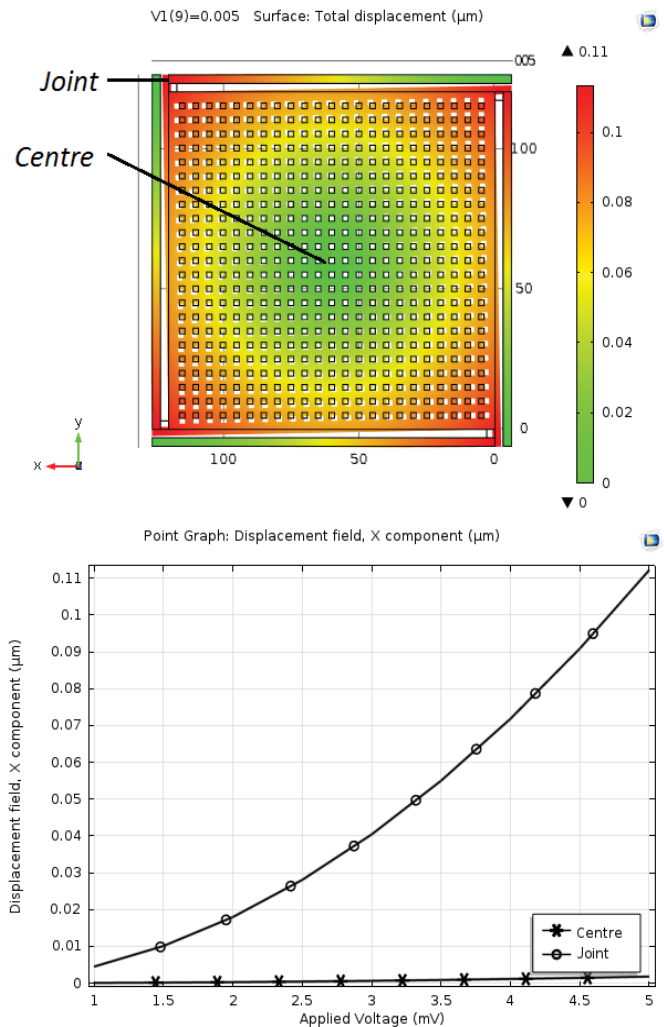


Fig. 11. Thermal expansion displacements (centre and beam joints).

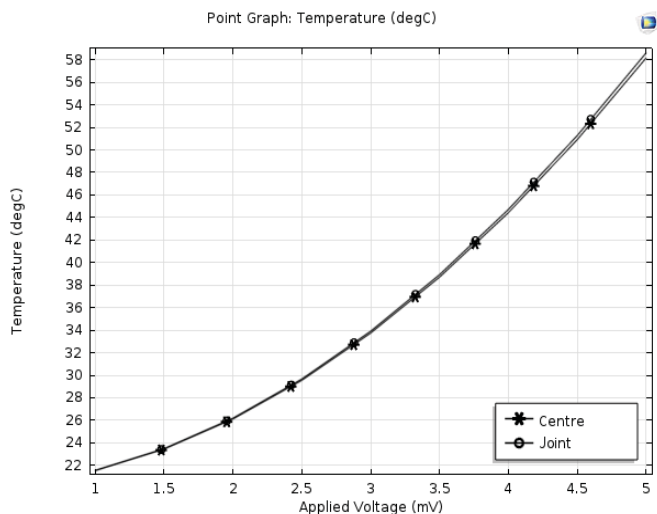


Fig. 12. Temperature rising (centre and beam joints).

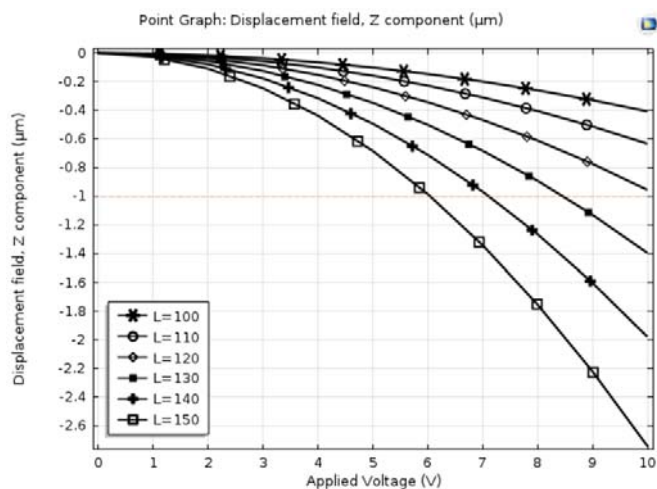


Fig. 13. Displacement as a function of voltage.

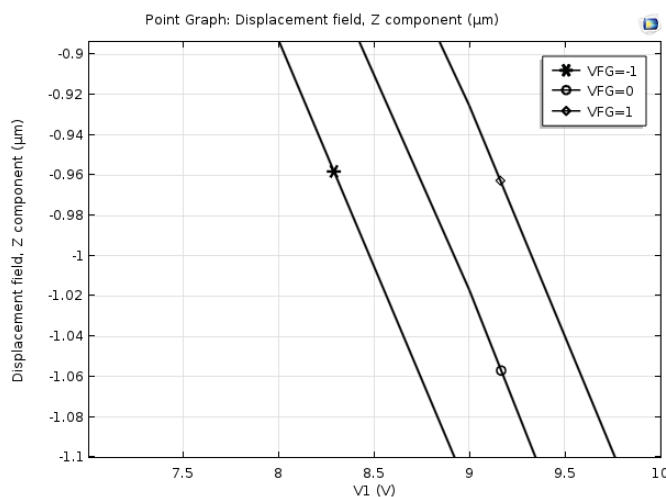


Fig. 14. Displacement being affected by floating-gate potential.

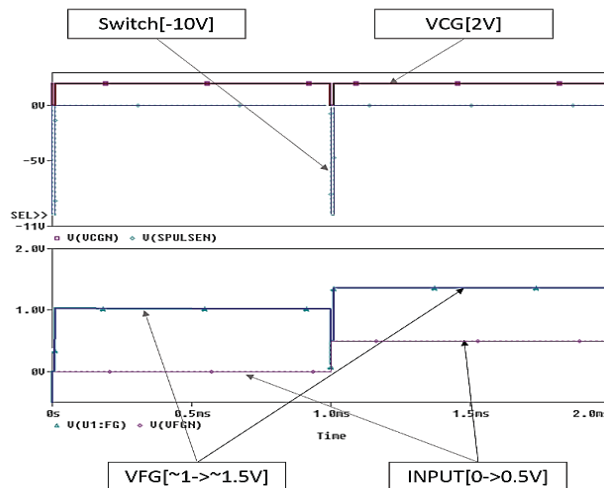


Fig. 15. Biasing scheme and coupled potentials superposition.

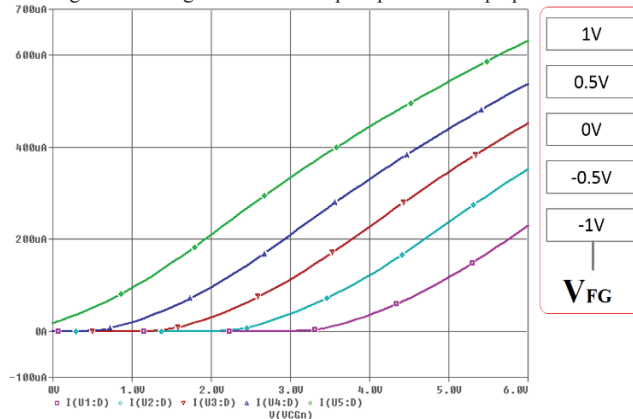


Fig. 16. Transconductance characteristic of an N-type FG-MOSFET.

V. CONCLUSIONS

The 0.5-micron standard CMOS technology was proven suitable for the development of capacitive MEMS structures and the non-overlapping biasing scheme is shown to be a reliable method for quasi floating-gate MOSFET applications.

The mere implementation of an electromechanical switch provides a much higher isolation for DC signals in comparison with the solid-state MOSFET switch usually found in quasi floating gate systems. Also, this work sets a basis for a highly linear capacitive transducer that can be used in fully-floating applications by coupling capacitive potentials instead of having a metal-metal contact in the membrane.

Furthermore, although this work is focused in design and simulation issues, for fabrication concerns an overglass layer window and further etching procedures must be considered in order to complete the structure.

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