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A simple method for determination of Fowler–Nordheim tunnelling parameters

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A simple technique for extracting the Fowler–Nordheim (FN) tunnelling parameters is proposed. It consists of measuring the Drain-Source current of a floating gate transistor while a linear ramp voltage is applied to a simple injector structure attached to the transistor's floating gate. Such a test device is fabricated using a standard CMOS process. The parameters obtained can be used in a freely available electrical simulator as SPICE3f5 (NGSPICE), but in general it can be easily adapted to other SPICE-like programs. We describe the technique step-by-step and a comparison is made of simulated and measured FN tunnelling parameters, for a floating gate transistor with tunnelling injectors. A good agreement has been found between experimental and simulated data.

Keywords: analogue circuits; CAD; semiconductors; measurements; integrated circuits; Fowler–Nordheim tunnelling

1. Introduction

Values for Fowler–Nordheim (FN) tunnelling parameters, α and β, are important in the simulation of circuits where floating-gate transistors (FGMOS) are used, as they are related to artificial neural networks, pattern recognition circuits, offset trimming, etc. The determination of FN parameters is still under discussion, contributing to the extraction of theoretical and experimental parameters. Circuit simulation is an important issue within integrated circuit design, and therefore modelling of the different carrier injection methods used in digital and analogue memories is also important. Among these injection methods, FN carrier tunnelling is currently used in non-volatile memories or adjustable synapses in artificial neural networks, for instance. However, specifically with FN tunnelling, some difficulties can be found in extracting α and β such that they can be characterised and then included into the library of a given circuit simulator. As reported by Harabech, Bouchakour, Canet, and Sorbier (2000), Chiou, Gambino, and Mohammad (2001) and Croci, Plossu, Balland, Raynaud, and Boivin (2001), FN parameters are influenced by factors such as injection oxide thickness spread, substrate doping type, gate structure, gate geometry, injection area and measurement conditions as well. These facts drive the necessity to extract parameters from a particular technology among those offered by silicon foundries. Our intention is to report a different methodology that facilitates parameter extraction using test structures

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fabricated by one of these silicon foundries, instead of large area capacitors issued in research laboratories, having technology processes different from those used in standard fabrication of integrated circuits. Here, the extraction methods are rather complex since the model used is based on several fitting experimental data as flat band voltage, Si/SiO_2 interface density states, substrate and gate doping level and electron effective mass. On the other hand, modelling and parameter extraction can be actually done with costly dedicated software. In the present work, an FN parameter extraction methodology and a model for FGMOS devices are reported that can be applied into a freely available electrical simulator. It is important to remark that the usual method applied for FN tunnelling parameters extraction is based on measurement of the current flowing through a large area MOS capacitor (Harabech et al. 2000). Since the tunnelling current density is very small, a large injection area is needed, so that injection current can be directly measured. This method could introduce undesirable effects if the area of the capacitor is large, since a high series resistance is introduced causing a deviation from the typical tunnelling current density model for FN injection, so a more complex model should be used for a reliable characterisation of the tunnelling parameters (Miranda 2008). Other methods use a floating-gate NMOS (FGMOS) transistor with an injector, to which a square-shaped voltage pulse is applied for adding/extracting charge to/from the floating gate, followed by the measurement of the threshold voltage of the FGMOS. Using this measured value together with the corresponding FGMOS transistor's capacitive model, the added/extracted charge can be estimated. Hence, the mean tunnelling current can be calculated using this charge and the pulse width of the applied voltage at the injector. This way, when several pulses are applied to the injectors of the floating-gate transistor, data can be obtained from measurements that can be properly plotted as a line, in order to derive α and β using linear regression techniques. Other studies (Saillet et al. 2006) use the I_D versus V_D measurement through an MOS dummy cell to extract the FN parameters, but no specification of the characterisation procedure is established. Another option is to continuously measure the drain current while charge is injected to a floating-gate of a FLOTOX memory cell, as reported in Larcher, Pavan, Gattel, Albani, and Marmirolli (2001) and Laffont et al. (2003). We agree with the basic idea but what we propose is a different approach. First, as an initial condition, the device under test (N-channel FGMOS) is programmed until a 10×10^{-6} A drain current is present with a zero control-gate voltage, thus the floating gate potential is positive. Then, if a positive/negative linear ramp pulse is applied to the injector to extract/inject charge from/to the floating gate, it is observed that the drain-source current will first change smoothly while the voltage across the injector in not enough to activate FN tunnelling. As soon the voltage of the ramp reaches a critical voltage across the injector, the effects due to the tunnelling can be identified. We develop a procedure for determining FN parameters from the measurement of the voltage ramp applied to the injector and together with the drain current flowing through the FGMOS, based in a well differentiated zone from an I_{DS} versus t plot, where the tunnelling effect is evident. To demonstrate this, we also develop a simple model to be used in the simulation of the I-V characteristics of an FGMOS with a couple of injectors: one for extraction and the other for injection. Such a structure was fabricated using a standard CMOS process available from MOSIS. The model is described in Section 2 and the FN parameter extraction procedure is depicted in Section 3. Then, the experimental setup is described in Section 4 followed by the results and discussion in Section 5, ending with the conclusions in Section 6.

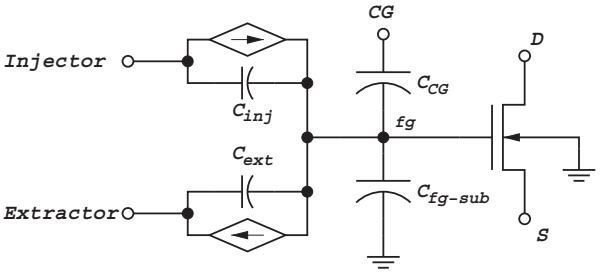

Figure 1. Equivalent circuit for an FGMOS transistor with structures for injection and extraction of charge to/from the floating-gate.

2. Simulation model

Our test structure is very simple (Figure 4). It has minimal gate-source and gate-drain parasitic capacitances, besides fixed voltages are applied to the FGMOS source and drain terminals (zero and +5 volts, respectively); thus, voltage feedthrough can be neglected. Furthermore, an FGMOS with the former initial conditions proposed ($I_{DS}=10\times10^{-6}$A, $V_D=+5$V, $V_S=0$V, $V_G=0$V) is operating in strong inversion, so depletion capacitance under the gate has no effect either. As a consequence, a simplified fixed-capacitances model can be used for the simulation of the device, as shown in Figure 1. The FGMOS equivalent circuit includes two injectors, represented by capacitors labelled C_{inj} and C_{ext}. The first one is for adding charge and the other is for removing charge, to/from the floating-gate. The last one will be called extractor from now on. A voltage-controlled current source is placed between C_{inj} and C_{ext} to simulate FN tunnelling, in the appropriate direction, according to

$$I = A\alpha\left(\frac{V}{d}\right)^2 \exp\left(-\frac{\beta d}{V}\right), \tag{1}$$

where the electric field has been replaced by V/d, A is the tunnelling area, d the tunnelling oxide thickness and V the voltage across the injector. C_{CG} is the capacitor between Control-Gate (CG) and floating-gate and C_{fg-sub} the parasitic capacitance between floating-gate and the substrate. In our simulations, the substrate and the CG terminals are grounded, and therefore their feedthrough voltages are zero. C_{OX} is not illustrated since it is included in the BSIM3 model and is taken into account already when a simulation is carried out. Other models as those developed by Saillet et al. (2006) and Maure, Canet, Lalande, Delsuc, and Devin (2008) use dedicated software such as ICCAP for parameter characterisation and ELDO for the model simulation, so the method is rather restricted to these tools. On the other hand, the models reported in Larcher, Pavan, Pietri, Albani, and Marmirolli (2002) and Kang and Hong (2005) are also good alternatives, but they do not use FN parameters, they rather use fitting parameters to adjust the I-V behaviour of the devices. The simulation with the model proposed in this work was done using a freely available simulator called NGSPICE which is an enhancement of Berkeley-Spice3f5. Figure 2 shows the plot of I_{DS} and V_{PP} from a transient simulation of the FGMOS using the elements shown in Figure 1, where a positive linear ramp voltage with a slew rate of 1000 V/s is applied to the extractor terminal and the injector terminal is connected to the ground. For this simulation, the following values were used for the voltage controlled

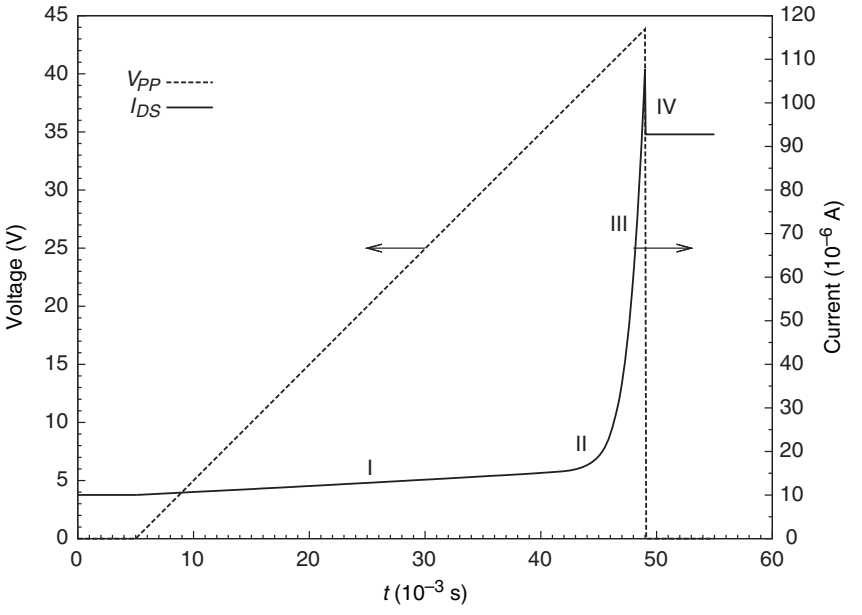

Figure 2. Simulation of extracting charge from FGMOS transistor's floating-gate.

current sources (Equation 1) to consider the FN phenomenon: $\alpha = 1.25 \times 10^{-6}\,\mathrm{A\,V^{-2}}$, $\beta = 2.67 \times 10^{8}\,\mathrm{V\,cm^{-1}}$, $A = 1.0 \times 10^{-4}\,\mathrm{cm^2}$ and $d = 50 \times 10^{-7}\,\mathrm{cm}$. This thickness was adjusted in order to obtain a smooth increase in the drain current of the FGMOS under tunnelling condition, so this phenomenon could be easily characterised. The complete simulation statements are found in Appendix A. Also in Figure 2, four regions can be well distinguished: (I) I_{DS} presents a slight linear increase due to the charge induction into the floating-gate through the extractor capacitance; since this capacitance is very small, the coupling coefficient reflects only a little fraction of the programming voltage and its effect can be neglected; (II) when FN tunnelling begins, a 'knee' is observed; (III) a very fast I_{DS} increase can be seen due to the change in the floating-gate voltage, that depends also on the induced charge by the programming voltage and the presence of a high tunnelling current dominating over the first one. This behaviour is suddenly stopped when the ramp is changed to zero; (IV) since the extractor voltage at this stage is zero, the value of the drain-source current is now determined only by the charge present upon the floating-gate so I_{DS} decreases once the ramp voltage goes to zero.

3. FN parameter extraction procedure

From the data used in Figure 2, the FN parameters are extracted as follows:

(i) Choose a set of points (t, V_{PP}, I_{DS}) from region III (where high tunnelling exists), between the border of regions II–III and just before V_{PP} goes to zero.
(ii) For every point selected, find the corresponding floating-gate voltage V_{fg}. This task is immediate since the simulation results include such values. Experimentally, we have no opportunity to measure the floating-gate potential

directly, so we need to map every I_{DS} value from the FGMOS to the transconductance curve of a dummy or reference transistor, which is identical to the FGMOS but with the Control-Gate and the floating-gate short-circuited.

(iii) Compute tunnelling voltage values at every point

$$V_{tun} = V_{PP} - V_{fg}. \tag{2}$$

(iv) Compute floating-gate voltage due to charge trapped only

$$V_{fg}^{Q} = V_{fg} - V_{PP} \times \alpha_{inj} \tag{3}$$

and knowing that α_{inj} is the coupling coefficient for the injector or extractor capacitor given by

$$\alpha_{inj} = \frac{C_{inj}}{C_{CG} + C_{fg-sub} + 2C_{inj} + C_{OX}}. \tag{4}$$

(v) Calculate the charge injected/extracted to/from the floating-gate by FN tunnelling between consecutive samples

$$\Delta Q_{fg}^{FN} = \frac{V_{fg}^{Q}(t_n) - V_{fg}^{Q}(t_{n-1})}{C_{CG} + C_{fg-sub} + 2C_{inj} + C_{OX}}. \tag{5}$$

(vi) Mean tunnelling voltage between consecutive samples can be approximated by a square-shaped voltage pulse whose amplitude is given by

$$\overline{V_{tun}} = \frac{V_{tun}(t_n) - V_{tun}(t_{n-1})}{2}. \tag{6}$$

(vii) Mean tunnelling current between samples is determined by

$$\overline{I_{tun}} = \frac{\Delta Q_{fg}^{FN}}{t_n - t_{n-1}}. \tag{7}$$

(viii) Finally, plot the data obtained from the last two steps as $\ln(I_{tun}/V_{tun}^2)$ versus $1/V_{tun}$. The FN classical behaviour is obtained. Doing a linear regression, α and β can be determined from the *y axis* intercept b and slope m, respectively,

$$\alpha = \frac{b}{A}, \tag{8a}$$

$$\beta = \frac{m}{d}, \tag{8b}$$

where A is the tunnelling area assumed to be the whole injector/extractor area and d is the tunnelling thickness between the polysilicon layers.

Theoretical calculations of FN parameters were done within the next time interval: $47.5 \times 10^{-3} - 49.0 \times 10^{-3}$ s with 25×10^{-6} s steps. Using our procedure, Figure 3 was obtained, where linear regression was done in order to extract FN coefficients. The values extracted were 1.24789×10^{-6} A V^{-2} for α and 2.56904×10^{8} V cm^{-1} for β, which are very close to those used for simulation. It can be seen that for the time range selected, the theoretical derivation of α and β follows a completely straight line, as the FN model predicts for this kind of a plot.

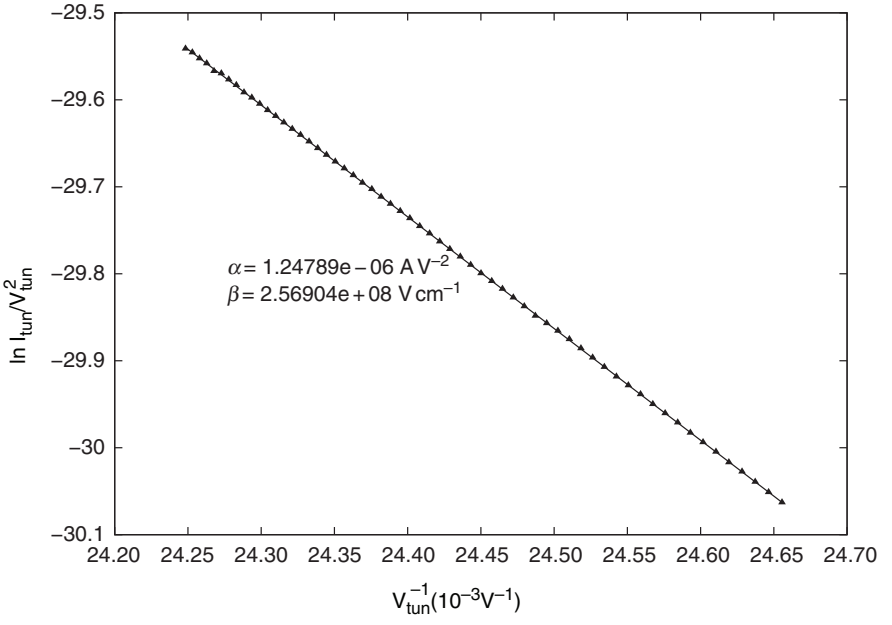

Figure 3. FN plot for data taken from simulation showing tunnelling coefficients values extracted using the proposed methodology.

4. Experimental setup

The FGMOS cell characterised in this work was fabricated using a standard Double Polysilicon CMOS process – MOSIS AMIS-ABN 1.6 μm – which includes a well-known simple injector structure which has been studied extensively. The cell layout is shown in Figure 4 and it is important to notice that although the injectors are just an overlap of Polysilicon2 and Polysilicon1 minimum width strips, the injector electrode structure connected to the floating-gate is not similar. Ideally, the FN parameters should be equal and independent of the electric field direction, but several works using diverse technologies, have reported a kind of geometric or surface texture dependence of the FN parameters values, since injection parameters were different from the extraction ones. In our case, for the technology used, it was found that only the emission from Polysilicon2 to Polysilicon1 was present with the voltage range used herein. Tunnelling emission in the opposite direction did not take place even with voltages as high as 60 V, so the injector whose Polysilicon1 electrode is connected to floating-gate was used for adding charge when a negative pulse is applied to the Polysilicon2 electrode. On the other hand, for charge extraction, the floating-gate is connected to the Polysilicon2 electrode, so charge will be extracted when a positive pulse is applied to the Polysilicon1 electrode. For the technology used, the oxide thickness between the Polysilicon1 and Polysilicon2 layers is 61×10^{-9}m, this value was calculated from the technology data provided by MOSIS for the fabrication process. A dummy cell or Reference Transistor, with similar layout but with the control-gate and the floating-gate short-circuited, was also fabricated.

Figure 5 shows the experimental setup used. It consists of an FGMOS like the one described above, a current-to-voltage converter, built around an AD711 operational amplifier, which is used for monitoring the I_{DS} current. This device has an input bias

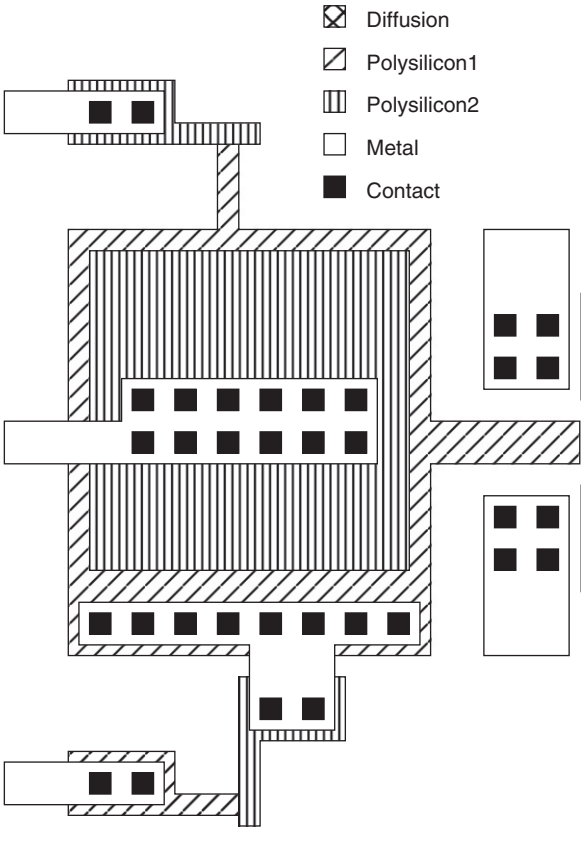

Figure 4. FGMOS layout for FN coefficients determination.

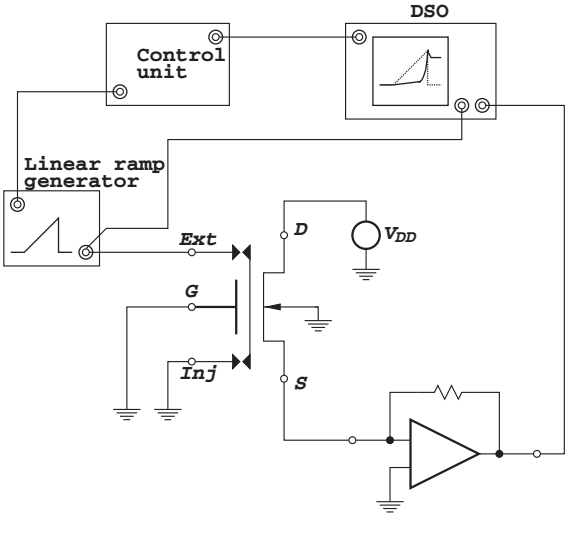

Figure 5. Experimental setup for extracting FN parameters.

current in the order of 10^{-12} A at room temperature, as a consequence, it does not load the FGMOS source terminal which is virtually grounded. The setup is completed with a DC power supply (V_{DD}), a Linear Ramp Generator with an external-trigger input, a Tektronix Digital Storage Oscilloscope (DSO) model TDS2020 with GPIB interface to read data from the instrument and a Control Unit to synchronise the last two. V_{PP} and I_{DS} are then captured by the oscilloscope. It is well known that the FGMOS, as fabricated, has random charge on the floating-gate as delivered from the silicon foundry, so it is recommended to program the transistor until a 10×10^{-6} A current flows from source to drain with a bias of $V_{DD} = 5$ V and $V_G = 0$ V, in order to comply with the conditions stated in Section 2. This can be done by applying short pulses with the correct polarity and amplitude to inject or extract charge to/from the floating gate. In order to have close control over the charge upon the floating gate, it is recommended to trigger once a chain of few pulses, until the desired I_{DS} current is obtained. Then, the Control Unit is triggered manually and it generates two pulses, one for triggering the Oscilloscope and one to begin a linear voltage ramp with a slew rate of $1000\,\mathrm{V\,s^{-1}}$ which is applied to the extractor. With the desired conditions settled, the evolution of I_{DS} and the exciting voltage ramp through time, can be measured with a digital oscilloscope, with the results illustrated in Figure 6(a).

5. Experimental results and discussion

Figure 6 shows the measurement results applying the method outlined in Section 3 and using the setup described in Section 4. Figure 6a shows the programming voltage and the current flowing through the measured FGMOS. The experimental results show that the four regions described earlier can be clearly distinguished. Figure 6b shows the graph for $\ln(I_{tun}/V_{tun}^2)$ versus $1/V_{tun}$, from which α and β can be easily obtained. The extracted values of α and β from this experiment are then used in the simulation of a tunnelling process. The result is plotted in Figure 7 along with the experimental curve. The value measured for α is 2.96877×10^{-10} $\mathrm{A\,V^{-2}}$ and for β is $6.49587 \times 10^{7}\,\mathrm{V\,cm^{-1}}$. Good agreement between simulation and the experimental curves is appreciated. Some differences can be found regarding the values reported for both parameters. Different values of β are reported, and this is attributed to the uncertainty of the oxide thickness (Chiou et al. 2001), injector's area and geometry, substrate doping type and level, tunnelling oxide properties, etc. (Croci et al. 2001). These technology parameters are particular for each silicon foundry and circuit designers have no influence on them. Theoretically, charge emission is bidirectional, i.e. from injector toward floating-gate and vice versa. However, this did not happen with our test structure and this was the reason why two structures were designed, as mentioned above, since charge emission was present only from Polysilicon2 toward Polysilicon1. A comparison between several values of β and the one obtained here is presented in Table 1. It should be noted that β has a strong influence on tunnelling current density, since it is the parameter within the exponential term in the FN tunnelling current density model. Then a small variation of β will result in a large variation of the tunnelling current. Therefore, a variety of values for β are still found in literature. Values of α can also have some differences due to measurement conditions and the kind of gate oxide processing (Chiou et al. 2001) as well as to a non-uniform electric field across the emitting surface (Nicolaescu and Nagao 2003). The α value is quite uncertain because we are considering the total extractor area as the tunnelling area. Contradictions can be found regarding the

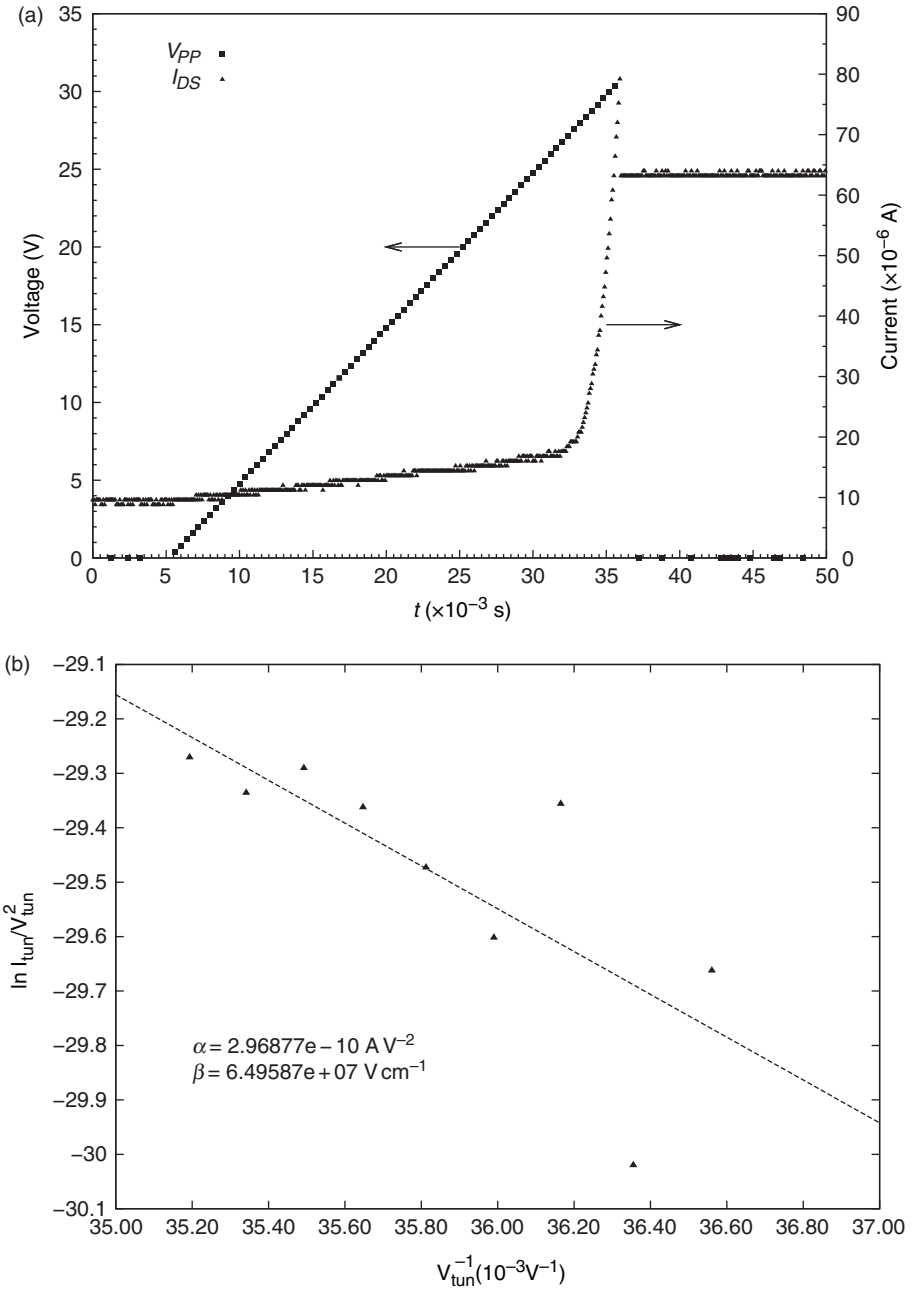

Figure 6. (a) Linear ramp pulse applied to the FGMOS extractor and drain-source current that flows through the transistor. (b) Plot made from calculated tunnelling voltages and currents for extracting FN parameters.

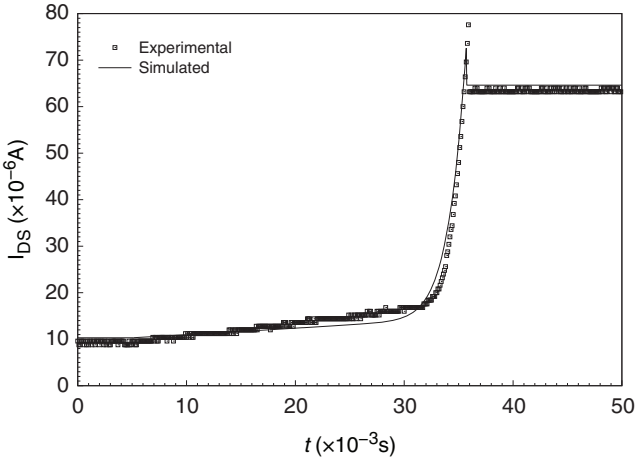

Figure 7. Comparison of source-drain current variation due to FN tunnelling. Square-shaped points are used for measured data and a solid-line for simulated data.

Table 1. Comparison between the β parameter value obtained by different authors and the one obtained using our procedure.

β (10^6 V cm^{-1})	Authors
255	Kolodny, Nieh, Eitan, and Shappir (1986)
223	Bez, Cantarelli, and Cappelletti (1990)
188	Keeney et al. (1992)
267	Gao and Senelgrove (1994)
251	Kosaka, Shibata, Ishii, and Ohmi (1995)
258	Chiou et al. (2001)
218–283	Croci et al. (2001)
65	Present work

influence of the injection area upon the value of α. Chiou et al. (2001) suggests that this parameter can be affected by the uncertainty of the contact area, while Brown, Collins, and Marshall (1995) and Croci et al. (2001) concluded that the tunnelling parameters do not depend on gate area. Moreover, it has been shown that the emission area value depends on the applied voltage (Forbes and Jensen 2001) and for the kind of injector we use, where oxide thickness is considered to be thick, electron emission takes place along injector's borders. Therefore, there is work to be done towards the definition of this behaviour. The extraction methodology can be improved using high resolution instrumentation for data acquisition, in order to have less dispersion in data reading.

6. Conclusions

We have demonstrated a technique for obtaining the Fowler–Nordheim tunnelling parameters. The values obtained using this method were used in a very simple SPICE

model that can be easily included in a library of a freely-available SPICE simulator. Close agreement between theory and experiment was obtained, which validates our parameter extraction procedure and simulation model. This technique can be very useful in characterising standard integrated circuit technologies and the model can be used in the simulation of floating gate devices through free access software for those who do not have access to special IC fabrication processes (thin oxides, low doped drain area) or a restricted simulator. Calculation improvements can be achieved using more accurate instruments like a 12- or 16- bits DSO which are not as expensive as professional semiconductor characterisation systems.

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Appendix: SPICE statements for FN tunnelling parameter extraction procedure

```
Fowler-Nordheim Tunneling Simulation

Vdd Vdd 0 DC 5V
VddAO VddAO 0 DC 12V
VssAO VssAO 0 DC -12V

VppOn VppOn 0 PULSE(5 0 5ms 10ns 10ns 44ms 55ms)
Epp Vpp 0 1 0 10
I1 0 1 DC 100u
C1 1 0 1u
XMpp 1 VppOn 0 2N7000

Btun Vpp 3 I=1E-4*1.25E-6*(abs(V(Vpp, fg))/50E-7)^2
+ *exp(-50E-7*2.57E8/abs(V(Vpp,fg)))
Vsenseitun 3 fg DC 0

Cg 0 fg 328.32f
Cpar fg 0 31.3344f
Cext Vpp fg 1.4592f
Ciny 0 fg 1.4592f

Mcelda Vdd fg 2a 0 CMOSN W=4.8u L=3.2u Pd=35.2u Ps=35.2u
Vsenseids 2a 2b DC 0
Rsen 2b Sal 10k
RL Sal 0 10k
X1 0 2b VddAO VssAO Sal AD711

.include t81y.mod
.include ad711.mod
.include 2n7000.mod
.tran 25us 55ms
.ic v(1)=0 v(fg)=1.08
.end
```