Assessment of the Possibility to Couple a Photo Sensor to a Floating-Gate MOS Transistor.

Domínguez-Sánchez S.
CINVESTAV, Electrical Eng. Dept.
Solid State Electronics Sect.
Mexico City, Mexico
sdominguezs@cinvestav.mx

Reyes-Barranca M. A.
CINVESTAV, Electrical Eng. Dept.
Solid State Electronics Sect.
Mexico City, Mexico
mreyes@cinvestav.mx

Mendoza-Acevedo S.
Centro de Investigación en Computación
Instituto Politécnico Nacional
Mexico City, Mexico
smendoza@cic.ipn.mx

Nava-Flores L. M.
CINVESTAV, Electrical Eng. Dept.
Solid State Electronics Sect.
Mexico City, Mexico
lmflores@cinvestav.mx

Moreno-Cadenas J.A.
CINVESTAV, Electrical Eng. Dept.
Solid State Electronics Sect.
Mexico City, Mexico
jmoreno@cinvestav.mx

***Abstract*— This paper presents preliminary results from experiments directed to demonstrate novel approximations that can lead to new applications for Floating-gate MOS transistors (FGMOS). This device began to be used in the '60s in digital and analog configurations in a variety of reliable applications, either supported on the non-volatile or volatile property of this transistor. This is achieved by injecting/extracting charge to/from the floating gate through electrical mechanisms like Fowler-Nordheim Tunneling (FNT) or Channel Hot Electrons (CHE). This work shows that the same as with the mentioned mechanisms, I-V characteristics can also be modulated with physical rather than electrical phenomena, like the photonic one, among others. A simple amplifier configuration was used, using discrete components like a small solar cells module and an integrated photo sensor. After measurement of the corresponding transfer curve of the amplifier, a curve shift was obtained thanks to the V_{OC} generated in the discrete device after illumination of the components, giving support to the hypothesis considered in this work, which can lead to a research work where integrated FGMOS transistors can be coupled to an integrated photo sensor, using a standard CMOS technology.**

Keywords—FGMOS; photo diode; PSPICE simulation

I. INTRODUCTION

Since the Floating-gate MOS transistor (FGMOS) was first presented by Kahng and Sze in 1967 [1], it had a continuous evolution that is still going on in the present days. First, this device was mainly used for digital memory structures like EEPROM, EPROM and Flash memories, taking advantage of the non-volatile property which allows digital information to be stored permanently, although functions not having this storage property can be configured as well. However, in time, new applications were found also within the analog domain, as demonstrated by Intel who launched an artificial neural network (ANN) with training incorporated [2]. Even more analog applications of the FGMOS can be found in [3-8] demonstrating the great potentiality of this device. A key factor responsible for the boost in the use of FGMOS was the work reported by Thomsen and Brooke [9] who demonstrated that it can be fabricated with standard CMOS technologies which are available for academia and also research and development. They used Fowler-Nordheim tunneling (FNT) to program/erase the device taking charge to/from the floating gate which modifies the threshold voltage, depending on the amount of charge involved. This can be made also with Channel Hot Electrons (CHE) and both became the standard methods normally used to shift the threshold voltage of FGMOS, taking advantage that this charge can be kept over a large period of time without leakage. The present work reports an assay to extend the known properties of the FGMOS regarding the way the I-V characteristics of this device can be altered by phenomena different than the electric ones. This was first reported in [10] where a FGMOS was used as a transducer in a semiconductor gas sensor (SGS) based on "*chemical injection*" over the floating gate resulting from the byproducts of a chemical reaction between a sensitive thin layer like SnO_2 and a reduction or an oxidizing gas. Now, the purpose is to demonstrate that this property can be extended too using light, assessing some experiments made using discrete devices, but with the intention to further integrate a photo sensor with a standard CMOS technology, and its possible use as an active pixel sensor (APS). Also, work is being done to extend the properties of the FGMOS based in

978-1-5090-3511-3/16/$31.00 ©2016 IEEE

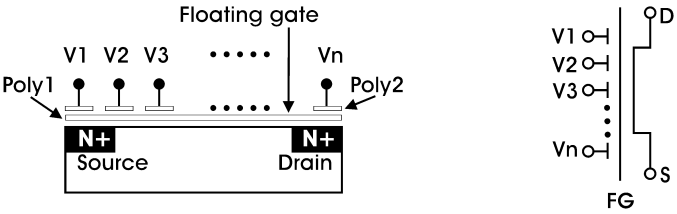
electromechanical and piezoelectric phenomena. The first one is based on a variable coupling coefficient, a concept that describes the electrical behavior of the FGMOS (MEMS accelerometer) and the latter, thanks to the voltage created due to an applied force over a piezoelectric material (quartz, barium titanate, etc.), as the device can be considered as a voltammetric sensor. It is worth mentioning that the gas sensor may have a non volatile property whereas the last considerations will be volatile since no charge is handled over the floating gate.

The way this paper is organized is described as follows: Section II gives a brief description of the FGMOS; Section III presents the expressions from which the photo sensors appear to be reliably coupled to an FGMOS; Section IV outlines the experimental procedure; Section V presents some preliminary results; and finally, Section VI presents the conclusions.

II. Description of the FGMOS Structure

The FGMOS is a device consisting in a completely isolated gate, surrounded with silicon dioxide, beneath a control gate which can have external electric access. In standard technologies, the floating gate and control gates are made with polysilicon layers called Poly1 and Poly2, respectively (Fig. 1a). More than one control gate can be configured, depending on the application and they are coupled to the floating gate with a coupling capacitor (Fig. 1b). Hence, a capacitive voltage divider is present with this capacitance array, such that the floating gate can be considered a sum node of the fractional voltages coming from each control gate. Therefore, a coupling coefficient, depending on the capacitance present all over the structure, determines the magnitude of the floating voltage present over the floating gate [9]. The capacitances present across the structure are C_{OX} (channel capacitance), C_{GD} (gate-drain overlapping capacitance), C_{GS} (gate-source overlapping capacitance), and C_{GB} (gate-bulk overlapping capacitance). Besides, there may be other parasitic capacitances also, that depend on the layout of the structure, but for simplicity only the array shown in Fig. 1b will be considered.

Considering a FGMOS with n control gates, if a transconductance I-V curve is generated with one of the control gates as reference, and if a voltage is applied over any of the other control gates, then the curve will be shifted to the left or to the right depending if this last voltage is positive or negative, respectively, as shown in Fig. 2. This figure plots the transconductance I-V curve for an n-channel FGMOS, but the same applies for a p-channel FGMOS. From here, it is supposed that voltages like the open circuit voltage of a solar cell (V_{OC}), or the voltage produced when a mechanical force is applied between the faces of piezoelectric compounds, are present over one of the control gates, this will have the same effect if they can be coupled to the floating gate with a coupling capacitor. So, this is the cornerstone that gives reason to begin this research, but limited exclusively to the photovoltaic response, although there is work in process regarding considering also stimulus either of chemical, mechanical or piezoelectric nature.



(a) (b)

Fig. 1. Floating-gate MOS transistor with n-gates. a) simplified cross section; b) schematic symbol

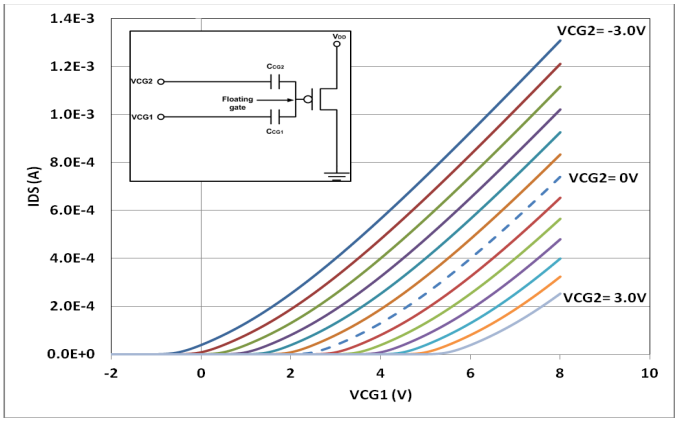


Fig. 2. Transconductance curve of an n-channel FGMOS with two control gates.

III. Photovoltaic Basis for the Implementation

From the macroscopic point of view, solar cells are p-n junctions made with a semiconductor substrate, Si for instance, that can generate a photo current proportional to the incident power of light. The equivalent circuit for a solar cell is shown in Fig. 3, where I_{PH} is the photo current generated, I_D is the current through the diode, C_j is the p-n junction capacitance, R_{SH} is the shunt resistance, and R_S is the series resistance [11].

Besides, the I-V characteristics of an ideal solar cell can be modeled with equation (1):

$$I = I_S - I_0\left(e^{\frac{qV}{mkT}} - 1\right) \quad (1)$$

where I_S is the photo current generated, I_0 is the reverse saturation current of the diode, V is the voltage applied to the diode, m is the ideality factor of the junction, q is the electron charge, k is the Boltzman's constant, and T is the temperature of the diode. From (1), the short circuit current, I_{SC}, can be defined when V=0, and on the other side, the open circuit

voltage, V_{OC}, can also be defined when I=0. They are represented by (2) and (3), respectively.

$$I_{SC} = I_S \tag{2}$$

$$V_{OC} = \frac{mkT}{q} ln\left(1 + \frac{I_{SC}}{I_0}\right) \tag{3}$$

Then, from (3) it is clear that the open circuit voltage is defined when the current across the diode is zero, thus corresponding exactly to the condition of zero current when a voltage is applied to the gate of a MOS transistor. This is the voltage that is being considered in this work to prove if it can modify the I-V characteristics of the FGMOS when a photo sensor is illuminated. Moreover, although the conditions mentioned before were established for a macroscopic solar cell, the behavior is still valid for CMOS micro photo sensors as those commonly integrated with standard CMOS technology, and the purpose is to assess if the V_{OC} of an integrated photo diode can be coupled to the floating gate of the integrated FGMOS, where as can be seen in Fig. 1, the floating gate serves as a summing node when more than one control gate are added to the FGMOS. It is important to say that three kinds of photo sensors can be fabricated in a standard CMOS technology: n^+diffusion/p-substrate, p^+diffusion/n-well, and n-well/p-substrate [12,13].

Fig. 4 shows an I-V representative simulated response of a photo diode at different generated photo currents, where different V_{OC} values are obtained for each curve. This voltage is the one that is pretended to be coupled to the floating gate, and several experiments were conducted with discrete devices in order to evaluate the possibility to further integrate a photo sensor coupled with a FGMOS. The following sections present some preliminary results.

IV. Experimental Procedure

In order to prove the phenomenon explained before, a series of experiments were designed and performed, consisting on measurements made to circuits based on discrete devices. Electrical characterization was made using a Semiconductor Characterization System Model 4200 SCS, from Keithley; the circuit was mounted into a black box (15.5cmx9.5cmx5ccm) and illuminated with a LED about 2cm away from the photo diode. Fig. 5 shows the configuration of the simple amplifier used for this purpose, from which the transfer function was obtained to show the results. First, a photovoltaic solar module (see Fig. 6a) having a V_{OC}=4V and I_{SC}=100mA was used. Later, an integrated photo diode (see Fig. 6b) was used also (IXYS, model CPC1824, V_{OC}=4.5V, I_{SC}=100µA). Both were connected to the gate of two kinds of MOS transistors (discrete n-channel MOS BS170P, integrated n-channel MOS ALD 1106PBL). A ramp function from 0V to 5V was used as the input voltage of the amplifier, V_{IN}, and the output voltage, V_{OUT}, was recorded to show the behavior of the configuration in dark and with illumination. It is important to mention that two measurements were obtained as the orientation of the photo device was reversed for each one.

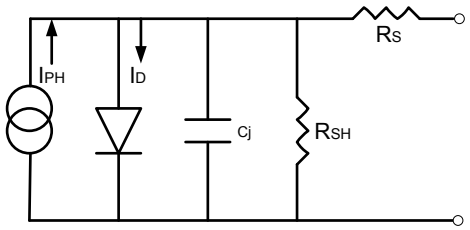


Fig. 3. Solar cell equivalent circuit.

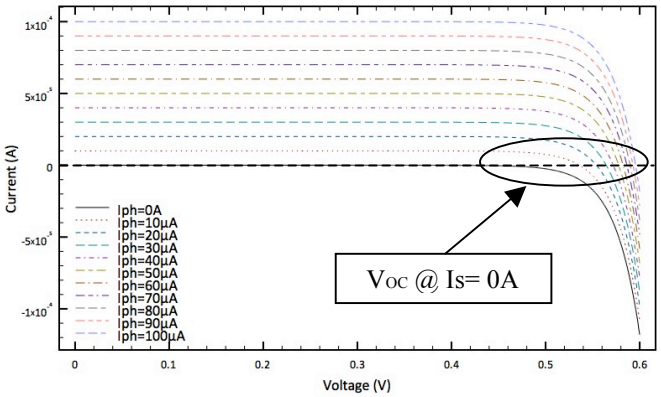


Fig. 4. Simulated I-V characteristic of a solar cell with different generated photo currents.

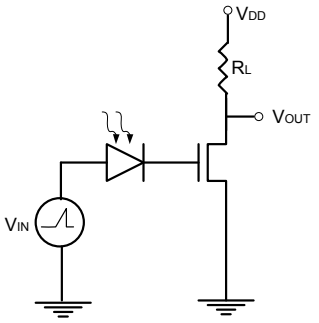
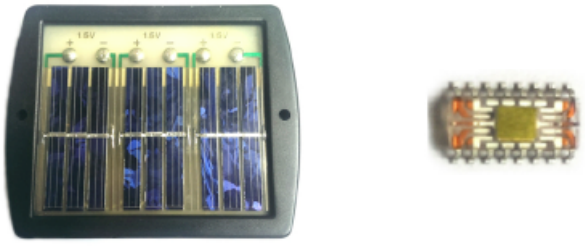


Fig. 5. Simple amplifier configured with a discrete photo devices and a MOS transistor.



(a) (b)

Fig. 6. Photo devices used for experimental measurements: a) Solar cell panel; b) integrated photo diode from IXYS.

Now considering the proposed integrated photo-diode connected to the control gate of a FGMOS, as shown in Fig. 7, a simulation with PSPICE was performed from which the response of the simple amplifier can be anticipated. The resulting transfer curve is shown in Fig. 8. Insets in this figure show the respective configuration considered when three photo-diodes are connected in series, applying a voltage sweep in V_{CG} with the incident power of light (Pin) as the parameter (0 to 5 µW/cm^2, with a 0.5 µW/cm^2 step).

V. Results and Discussion

The I-V characteristics of the IXYS integrated photo diode, in dark and illumination, are shown in Fig. 9 to show the experimental photoresponse of this device, where the magnitude of V_{OC} for each curve can be identified. The inset voltages correspond to different polarizations of an Ultrabright White LED VLHW5100 that is mounted within a black box where the array was connected, which gives different light intensities. Next, in Fig. 10 the transfer curve using the photovoltaic module is presented. Illumination was made with a 26 watts filament lamp.

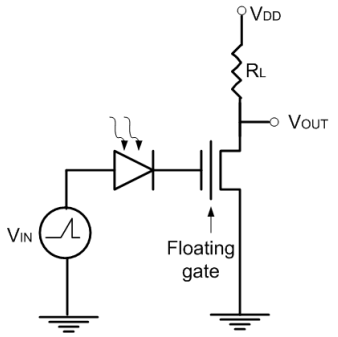


Fig. 7. Simple amplifier considering a FGMOS used for simulation with an input voltage sweep from 0 to 1.8V, with incident power of light (Pin) as a step (0 to 5 µW/cm^2, with a 0.5 µW/cm^2 step).

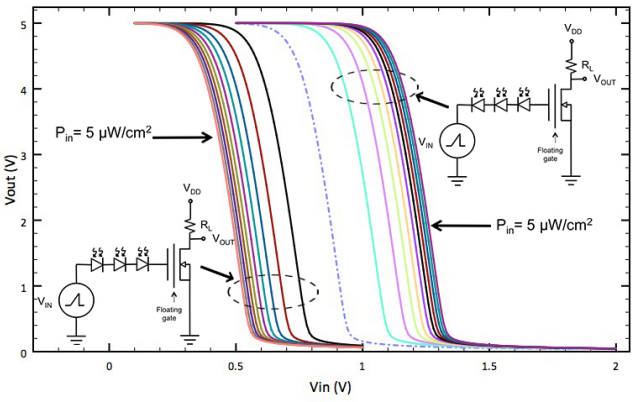


Fig. 8. Transfer curve resulting from the simulation considering the circuit shown in Fig. 7, using a FGMOS with three photo-diodes in series connected to the control gate.

Here it is confirmed that the expected behavior can be obtained, as anticipated with the simulation. Only one experimental curve is reported by now, but work is being addressed to obtain a family of curves depending on incident light power, as was obtained with simulation. From the experimental results, the curves that have a transition around V_{IN}=2V, correspond to the dark condition, whereas the curve whose transition is present at V_{IN}=5V results when the positive terminal of the module was connected to V_{IN} (ΔV= +3V) and the curve having its transition at V_{IN}= -1.5V, was obtained with the negative terminal of the module connected to V_{IN} (ΔV= −3.5V). A shift to the right of about 3V and to the left on the order of 3.5V was obtained with these configurations, which demonstrate at first instance, that the V_{OC} of this module can modulate the I-V characteristics of a MOS transistor when an illuminated photo sensor is connected to the gate of a MOS transistor. Since this paper reports an initial assessment of the behavior of the photo-diode connected to the control gate of a FGMOS, it is clear that a further work can be done in order to find a relationship between the incident light power and the curve shift, among several other parameters that must be characterized. Future tests could include even the kind and size of the integrated photo-diode and its optical characterization, and the size of coupling capacitances and laying out a proposal for a pixel for image processing, as well. Finally, Fig. 11 shows the same measurement but now using the integrated photo diode. Again, a curve shift of about −3.5V was obtained, after the structure was illuminated with the Ultrabright White LED. Here, only two curves are presented (in dark and illumination) since no trusted results were obtained when the anode was connected to V_{IN}, thus curves are only when the cathode is connected to V_{IN}. This may be thought since the data sheet of this device, which has a particular orientation within the chip, indicates that this array is capable of generating a floating source voltage, which can affect any reference during measurement. Anyway, similar results as those obtained with the solar cells module were obtained, giving strength to the hypothesis established above.

VI. Conclusions

It was shown, at a preliminary instance, that the photonic phenomena can have influence over the I-V characteristics of a MOS transistor and that it may be possible to extend this behavior to integrated FGMOS transistors. Although discrete components were used in this work, the effect of the voltage V_{OC} of a photo sensor can play the same role when integrated with CMOS technologies that offer two layers of polysilicon used commonly to fabricate FGMOS transistors. As the objective of this paper is to report the assessment of the hypothesis established, it is clear that further work must be done, directed to design test structures that can lead to confirm this preliminary results, giving an extension of the properties

of these kinds of devices. Promising results are being obtained actually and will be extensively reported in a future work.

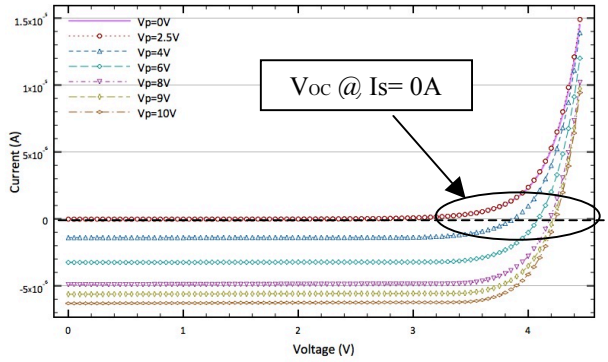


Fig. 9. Photoresponse of the IXYS photo diode.

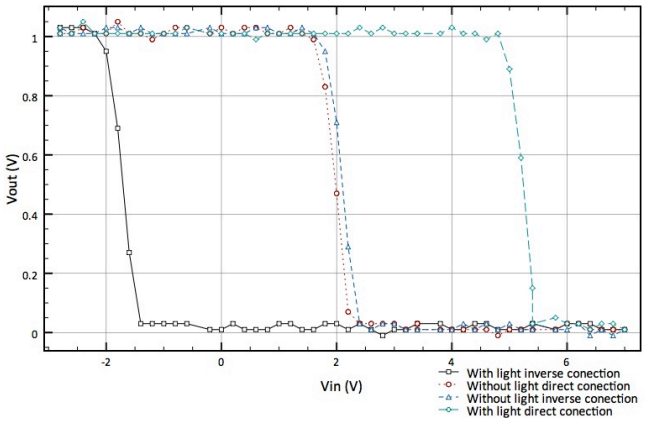


Fig. 10. Transfer curve of the configuration shown in Fig. 5, in dark and illumination, using the solar cell module.

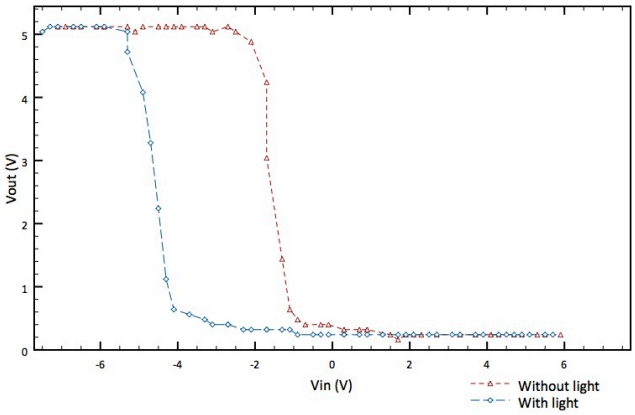


Fig. 11. Transfer curve of the configuration shown in Fig. 5, in dark and illumination, using the integrated photo diode.

REFERENCES

[1] D. Kahng and S.M. Sze, "A floating-gate and its application to memory devices", The Bell System Technical Journal, Vol. 46, No. 4, pp. 1288-1295, 1967.

[2] M. Holler, S. Tam, H. Castro, and R. Benson, "An electrically trainable artificial neural network with 10240 'floating gate' synapses", Proceeding of the International Joint Conference on Neural Networks, Washington, D.C., Vol. II, pp. 191-196, 1989.

[3] T. Shibata and T. Ohmi, "A functional MOS transistor featuring gate-level weighted sum and threshold operations", IEEE Transactions on Electron Devices, Vol. 39, No. 6, pp. 1444-1455, 1992.

[4] Fujita, O.; Amemiya, Y.; Iwata, A., "Characteristics of floating gate device as analogue memory for neural networks", Electronics Letters, Vol. 27, Issue 11, pp. 924 926, 1991.

[5] Liming Yin; Embabi, S.H.K.; Sanchez-Sinencio, E., "A floating-gate MOSFET D/A converter", Circuits and Systems, ISCAS '97, Proceedings of 1997 IEEE International Symposium on Volume: 1, 409 412, 1997.

[6] Lopez-Martin, A.J.; Ramirez-Angulo, J.; Carvajal, R.G., "Low-voltage FGMOS-based balanced current scaling in moderate inversion", 18th European Conference on Circuit Theory and Design, ECCTD 2007., 2007, pp. 56-59, 2007.

[7] Galán, J.; Lujan-Martinez, C.; Carvajal, R.G.; Ramirez-Angulo, J.; Lopez-Martin, Torralba, A., "Comparison of programmable linear resistors based on quasi-floating gate MOSFETs", ISCAS 2008, IEEE International Symposium on Circuits and Systems, pp. 1712-1715, 2008.

[8] Garcia-Moreno, E.; Isern, E.; Roca, M.; Picos, R.; Font, J.; Cesari, J.; Pineda. "A Temperature Compensated Floating Gate MOS Radiation SensorWith Current Output", IEEE Transactions on Nuclear Science, Issue: 99, pp. 15-28, 2013.

[9] A. Thomsen and M.A. Brooke, "A floating-gate MOSFET with tunneling injector fabricated using a standard double-polysilicon CMOS process", IEEE Electron Device Letters, Vol. 12, pp. 111-113, 1991.

[10] Reyes Barranca, M. A.; Mendoza-Acevedo, S.; Flores-Nava, L. M.; et ál. "Using a Floating-Gate MOS Transistor as a Transducer in a MEMS Gas Sensing System", Sensors, Vol. 10, No. 11, p.p. 10413-10434. Nov. 2010.

[11] S.M.Sze, Semiconductor Devices. Phisycs and Technology. 2nd Ed., John Wiley and Sons, U.S.A., 2002.

[12] M. Ferri, D. Pinna, E. Dallago, P. Malcovati, "Integrated Micro-Solar Cell Structures for Harvesting Supplied Microsystems in 0.35µm CMOS Technology"; IEEE Sensors 2009 Conference; p.p. 542-545, 25-28 Oct., Christchurch, New Zealand, 2009.

[13] Kartikeya Murari, , Ralph Etienne-Cummings, Nitish Thakor, and Gert Cauwenberghs; "Which Photodiode to Use: A Comparison of CMOS-Compatible Structures"; IEEE Sensors Journal, Vol. 9, No. 7, July, p.p. 752-760, 2009.