2019 16th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE)
Mexico City, Mexico. September 11-13, 2019

Composition of Metal Layers in CMOS-MEMS Micromachining Process

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Abstract – In this work some representative mechanical and materials-related issues in the design and fabrication of CMOS-MEMS devices are reviewed, especially those appearing in the further on-chip micromachining process needed to release MEMS structures within conventional CMOS integrated circuits.

CMOS-MEMS is a micro-sensor and micro-actuator development technique consisting in applying either an etching or deposition process to previously designed and fabricated CMOS circuitry, in order to enhance its mechanical, optical, chemical or so properties achieving a micro-electromechanical behavior.

In the case of material removal, also known as micro-machining, a surface or bulk process, usually a wet chemical etching, is used to release metallic structures embedded in insulating glass layers. Nevertheless, the composition of those metallic structures may vary from a CMOS fabrication technology to another and should not be neglected during the etching process.

Keywords – CMOS-MEMS, MEMS, Micromachining, Etching, Inertial, Sensor, TiN, Aluminum, Silicon dioxide.

I. CMOS-MEMS DESIGN

CMOS-MEMS is a set of techniques to develop sensors and actuators physically constructed at a very small scale within the silicon die where a CMOS integrated circuit is already fabricated. Generating microscopic mechanical structures is relatively easy taking advantage of the different material layers involved in the CMOS fabrication process. As presented in [1], technologies such as 0.5µm C5 from On-Semi, include up to three metallic depositions with typical thicknesses in the order of 1 micron, interleaved with SiO_2 layers for insulation, preventing from short-circuit issues during the interconnection between circuit modules.

These metal layers are generally thought to be an aluminum and copper (~5%) alloy, so for electronic design purposes the resistivity is considered to be similar to that of the pure aluminum, as well as its mechanical stiffness and temperature driven phenomena. Anyway, not every CMOS fabrication processes observes the same chemical composition for their metallic layers, actually, even a particular CMOS technology does not imply the same configuration for all of its layers. Most micro-sensors and micro-actuators form their mechanical structures out of the available metal layers and conveniently, whatever the functionality and geometry of the microsystem is, we may enumerate the metal layers as *Metal 1*, *Metal 2*, etc. from the bottom end (substrate) to the top as seen in Fig. 1. Also, to determine the approximate mass of a given metallic structure thickness must be considered. Table 1, as seen in [2] summarizes the structural parameters for the 0.5µm On-Semi conventional CMOS fabrication process.

Thickness of each layer and their respective mechanical stiffness takes especial relevance in inertial CMOS-MEMS sensor devices, since the electrical current parameter measured are closely related to capacitive variations from cantilever and mass-spring-like micro-systems.

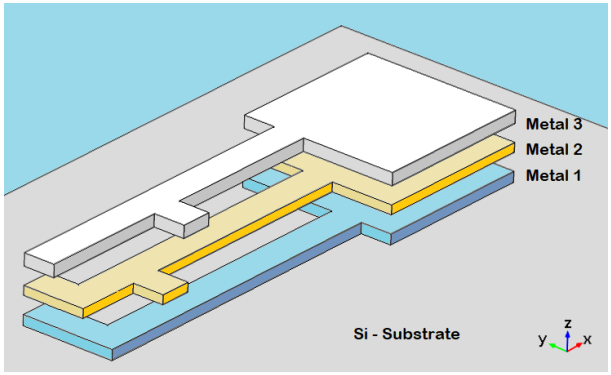

Fig. 1. 3-layer metal distribution in 0.5µm On-Semi process.

Parameter	Thickness [µm]
Metal 3	0.770
M2 to M3 dielectric	1.100
Metal 2	0.570
M1 to M2 dielectric	1.100
Metal 1	0.640
Field Oxide under M1	0.375

Table 1. Design parameters.

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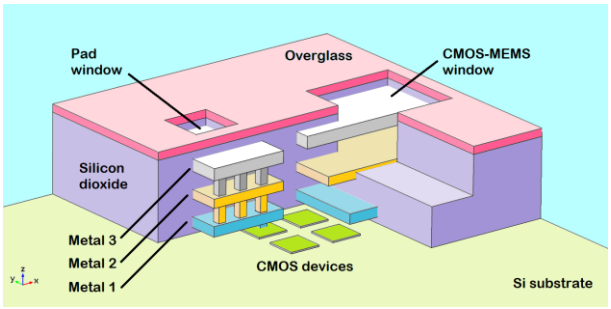

Fig. 2. Pad and micromachining windows.

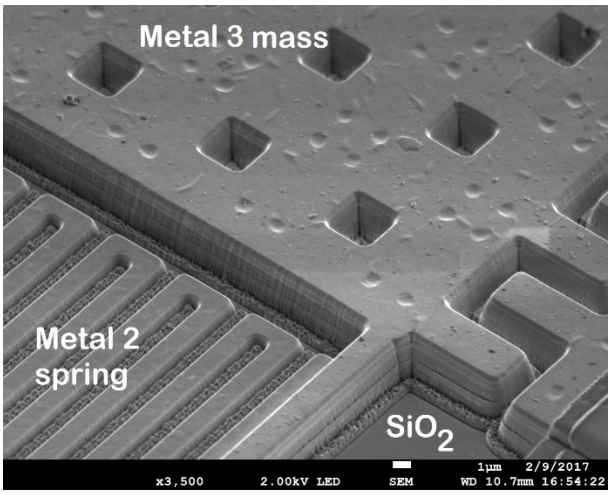

Fig. 3. Metal 2 and 3 structures in a custom overglass window.

Another topic to be considered is the way in which a brand new microchip is received from the foundry or vendor prior to execute an additional micromachining process. As can be seen in Fig. 2, CMOS devices remains at the crystalline silicon (Si) surface and a thick layer of silicon dioxide (SiO_2) is grown above. SiO_2 protects the electronic devices and insulates them from the metals above. By tacking multiple metal layers and linking them through via connectors a conductive path from the substrate to the exterior environment can be generated. The overall top layer on chip is a silicon nitride (Si3N4) deposition that covers all the chip, except where a pad window is requested by the designer so a wire can be bonded to the top metal. These pad windows has a standard size in every fabrication process and are opened through the overglass layer by means of a highly directional physical attack such as reactive ion etching (RIE). But also, designer is allowed to request custom-sized windows wherever it's needed and this is usually used to reach the lowest metal layers and release them from the embedding oxide by applying a further wet chemical substance which etch rate is quite higher for the silicon dioxide than for the silicon nitride, metal layers and the crystalline silicon substrate.

In Fig. 3 a chip with a custom window is shown and can be noticed that metal layers masks the RIE physical etch, and it is assumed that for a given process time, the silicon dioxide bulk was lowered down to a level about the Metal 2 layer. As said before, not every fabrication process has the same composition for the metal layers. The 0.5µm C5 fabrication process from On-Semi includes a titanium nitride platting [3] in its metallic layers. Since titanium nitride and aluminum work functions are quite similar (~4.5eV) [4] [5] [6] the main features of the TiN/AlCu/TiN stack are related to enhance Schottky devices and the mechanical protection of the layer itself. After an etching post processing, the existence of the substructures shown in Table 2 becomes more evident as can be seen in Fig. 4. May be highlighted that Metal 3 layer does not have an upper TiN cover. Silox Vapox III ®[7] was the applied SiO_2 etchant.

II. COMPOSITION OF METAL LAYERS

In order to select an effective chemical etchant and the appropriate process timing, the titanium nitride layer must be considered. The existence and properties of the titanium nitride plates were confirmed by means of three different techniques. First, in Fig. 5 an optical micrograph of metal samples within the fabricated integrated circuit is shown. The yellowish appearance of TiN in the Metal 2 sample can be easily noticed.

Parameter	Substructure (from the top)
Metal 3	AlCu / TiN
Metal 2	TiN / AlCu / TiN
Metal 1	TiN /AlCu / TiN

Table 2. Metal substructures.

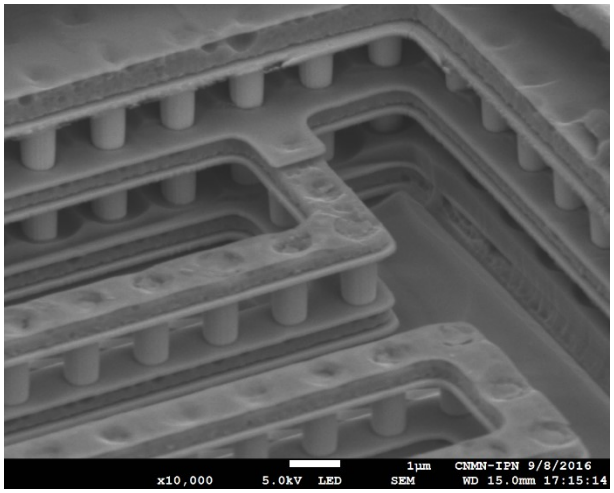

Fig. 4. All the three metal layers in C5 process after a wet etch.

Fig. 5. Metal and semiconductor layers micrograph.

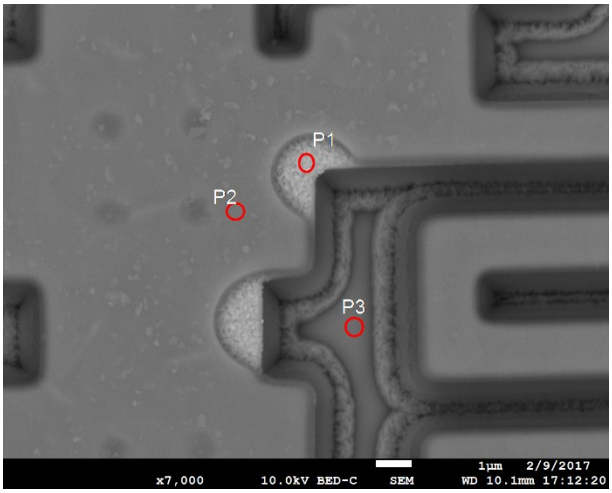

Fig. 6. EDS target points.

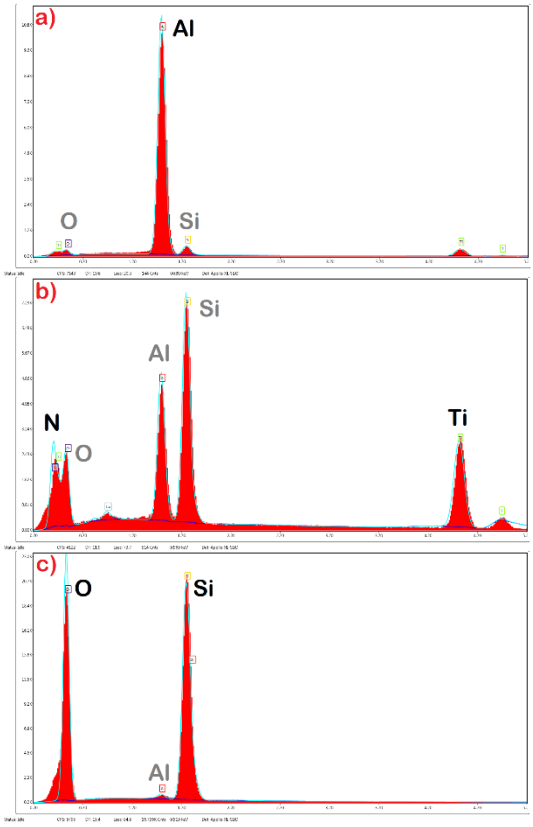

Fig. 7. EDS spectra.

Another characterization technique used to confirm the presence of titanium nitride was (besides to SEM) an Electron Dispersive Spectroscopy (EDS) analysis, pointing at three different regions in the integrated circuit. In Fig. 6 points P1, P2 and P3 are located on Aluminum, the TiN cover above and the subjacent silicon dioxide bulk, respectively. Fig.7 shows the EDS spectra for a) aluminum, b) nitrogen and titanium and c) oxygen and silicon components.

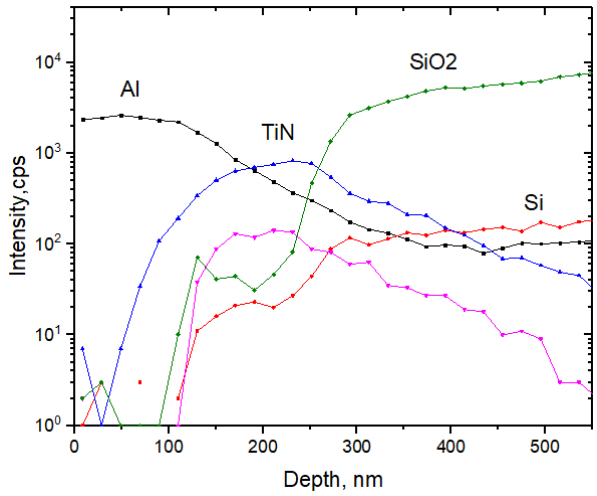

Fig. 8. SIMS profile.

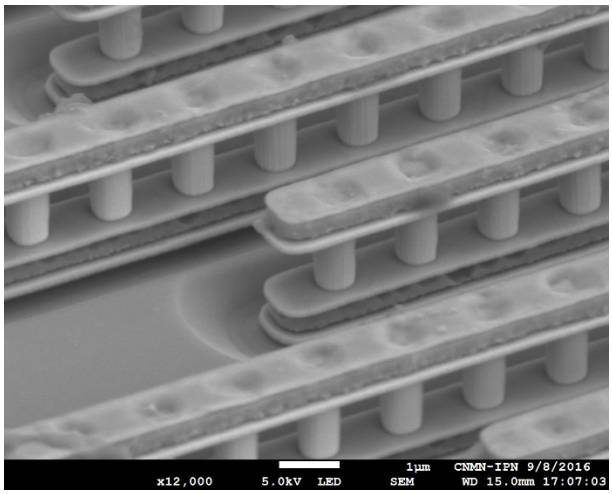

Fig. 9. Degraded Metal 2 layer.

Finally, in order to find the approximate TiN layer thickness a time-of-flight secondary-ion mass spectrometry (SIMS) analysis was performed on a Metal 3 sample. The SIMS profile shown in Fig. 8 confirms the Al/TiN/SiO_2 stack as it was expected and a TiN lower layer with a thickness in the order of 100nm can be appreciated.

III. POST-PROCESSING ISSUES

TiN has become an issue when it comes to micromachining based on a hydrofluoric acid (HF) solution, although etchant solutions such as Silox Vapox which are intended to have a very low aluminum etch rate and effectively removes SiO_2 bulk layers, most metallic structures were damaged in most of experimental results. In Fig. 9 (as well as in Fig. 4) the micrograph show what seems to be a TiN layer completely ripped off the Metal 2 – interdigital capacitor from [8] and [9]

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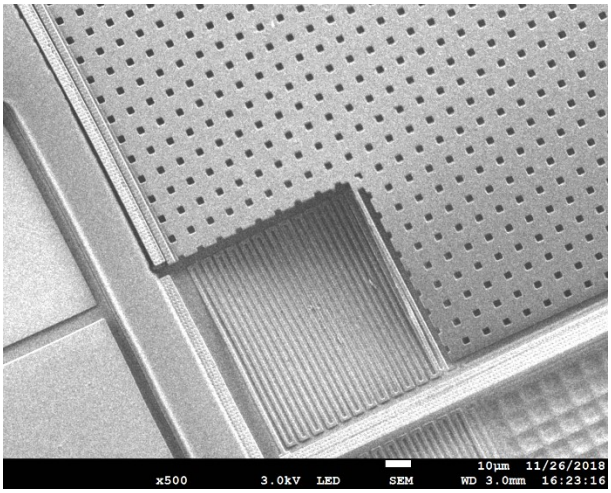

Fig. 10. Metal 2 - accelerometer proof-mass bending upwards due to stress.

(and spring beams in Fig. 4), since titanium nitride might not be rapidly dissolved in the HF solution, the strongest hypothesis suggest a poor adherence between metals. Another undesirable effect of the residual stress due to a differential stiffness is the deformation of relatively large structures (Fig. 10), such mechanical stress might be enough to fracture non-well supported beams and springs.

IV. CONCLUSIONS

CMOS-MEMS is a low-cost alternative to the MEMS traditional development processes which usually consists in wire-bonding two separated chips or silicon dice, one CMOS conventional integrated circuit and a micromechanical only device. Nevertheless the metal layers available in the MEMS chip are way thicker than those in the CMOS chip. This must be considered since CMOS-MEMS consists in the adaptation of a conventional CMOS chip.

The existence of a TiN layer covering the aluminum wires should be a major criteria to select a CMOS technology among a variety of choices. A process in which the metal layers are made up of pure aluminum would present better wet etch characteristics and in consequence a better overall performance.

TiN is a very versatile material but its use and properties a CMOS fabrication context are barely mentioned in literature, even vendors does not usually provide technical information about the fabrication. So this work might be considered as an inverse engineering exercise to improve future CMOS-MEMS design methodologies.

V. FUTURE WORK

As summarized in the present work, further comprehension of the mechanical properties of the TiN/AlCu heterogeneous compound would lead to both a new CMOS-MEMS design methodology and the consolidation of novel post-processing wet micromachining processes based in acid etchants.

ACKNOWLEDGMENTS

We would like to thank to the National Council of Science and Technology (CONACYT) and the VLSI Lab's community for the resources and advices given during the development of the present work.

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