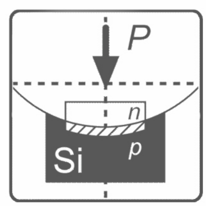
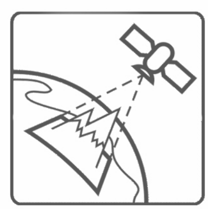
ADVANCES IN SENSORS: REVIEWS 5

Sergey Y. Yurish

Editor

# Physical Sensors, Sensor Networks and Remote Sensing



# Physical Sensors, Sensor Networks and Remote Sensing

Sergey Y. Yurish
Editor

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**Book Series: Advances in Sensors: Reviews, Vol. 5**

International Frequency Sensor Association Publishing

Sergey Y. Yurish
*Editor*

Physical Sensors, Sensor Networks and Remote Sensing
Advances in Sensors: Reviews, Vol. 5

Published by International Frequency Sensor Association (IFSA) Publishing, S. L., 2018
E-mail (for print book orders and customer service enquires): ifsa.books@sensorsportal.com

Visit our Home Page on http://www.sensorsportal.com



ISBN: 978-84-09-03028-6
e-ISBN: 978-84-09-03029-3
BN-20180730-XX
BIC: TJFC

**Acknowledgments**

As Editor I would like to express my undying gratitude to all authors, editorial staff, reviewers and others who actively participated in this book. We want also to express our gratitude to all their families, friends and colleagues for their help and understanding.

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# Preface

It is my great pleasure to present the fifth volume from our popular Book Series '*Advances in Sensors: Reviews*' started by the IFSA Publishing in 2012. Similar to the Vol.4, the Vol. 5 of this Book Series is also published as an Open Access Book in order to significantly increase the reach and impact of this volume, which also published in two formats: electronic (pdf) with full-color illustrations and print (paperback).

According to Allied Market Research (AMR), the global market of sensors and transducers is poised to grow with a compound annual growth rate (CAGR) of 11.3 % until 2022 when the market would reach US $241 billion. In the forecasted period, nanoelectromechanical systems (NEMS) are expected to be the fastest growers. It is expected also the main drivers to the overall sensor market will be IoT (smart homes, smart cities and intelligent vehicles), smartphones, automation (Industry 4.0), automotive and wearable. All these stimulate sensor research and development for appropriate vertical industries and applications. The publication of two volumes 5 and 6 of Book Series '*Advances in Sensors: Reviews*' in 2018 was an answer from the global sensor community to these challenges.

The Vol. 5 of this Book Series contains 22 chapters written by 79 contributors-experts from universities, research centres and industry from 15 countries: Australia, Canada, China, France, Germany, Italy, Malaysia, Mexico, Poland, Portugal, Russia, Slovenia, Spain, Ukraine and USA, who did also publish their research results in sensors related, established journals including 'Sensors & Transducers' journal published by IFSA. This volume contains information at the cutting edge of sensor research and related topics from the following three areas: Physical Sensors, Sensor Networks and Remote Sensing. Coverage includes current developments in various sensors, sensor instrumentation and applications.

In order to offer a fast and easy reading of each topic, every chapter in this volume is independent and self-contained. All chapters have the same structure: first, an introduction to specific topic under study; second, particular field description including sensing or/and measuring applications. Each of chapter is ending by well selected list of references with books, journals, conference proceedings and web sites.

With the unique combination of information in this volume, the *'Advances in Sensors: Reviews'* Book Series will be of value for scientists and engineers in industry and at universities, to sensors developers, distributors, and end users.

I hope that readers enjoy this new book volume and that can be a valuable tool for those who involved in research and development of various sensors and its applications.

I shall gratefully receive any advices, comments, suggestions and notes from readers to make the next volumes of *'Advances in Sensors: Reviews'* Book Series very interesting and useful.

*Dr. Sergey Y. Yurish*

*Editor*
*IFSA Publishing* *Barcelona, Spain*

# Chapter 12
# Gaussian Function Generator for a Perceptron ANN with FGMOS Transistors in an Integrated Circuit

**José Luis González Vidal, Mario Alfredo Reyes-Barranca and Edgar Norman Vázquez-Acosta**

## 12.1. Introduction

Floating gate transistors are a variant of conventional CMOS technology transistors (NMOS and PMOS), but FGMOS transistors have a polysilicon plate (isolated by layers of silicon oxide) between the channel area and the typical control gate (Fig. 12.1). Because the floating gate contains a charge, it influences the threshold voltage of the device. The relation between the threshold voltage and the floating gate parameters is explained in Eq. (12.1). Floating gate voltage $V_{fg}$ can be found by superposition, considering each of the voltages ($V_{cg}$ and $V_i$) applied to the structure, which is denoted in Eq. (12.1).

$$V_{fg} = \sum_i K_i V_i + K_{cgi} V_{cgi}, \tag{12.1}$$

$$K_i = \frac{C_i}{C_{tot}}, \tag{12.2}$$

$$K_{cg} = \frac{C_{pp}}{C_{tot}}, \tag{12.3}$$

where $C_{CGi}$ is the capacitance due to each of the *i* control gates, $V_{cgi}$ is the voltage applied to each control gate, $C_{tot}$ is the total equivalent capacitance, $V_D$ is the drain voltage, $V_S$ is the source voltage, $V_B$ is the bulk voltage, $C_{GD}$ is the parasitic capacitance between the drain and the floating gate, $C_{GS}$ is the parasitic capacitance between the source and the floating gate, $Q_{FG}$ is any residual charge that may be present on the floating gate, and $K_{cg}$ is defined as the coupling coefficient for each control gate. Therefore, it is clear that the

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drain current, $I_{ds}$, of the FGMOS will be a function of the floating gate voltage, which in turn, is a function of the injected charge present at the floating gate [1-4].

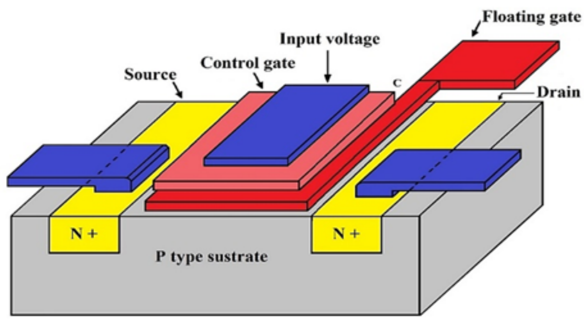


**Fig. 12.1.** FGMOS n-type.

This adaptability can be translated to electronic circuits and many algorithms were successfully implemented within electronic integrated circuits (IC) that attempt to emulate the neural biology behavior, based on assumptions derived from previous input values or new input values for training purposes of the ANN. Here, the element that can provide for the adaptability is the FGMOS, since it can deliver a variable resistance that can be adapted as is usual for typical weights used in several ANNs architectures.

As is well known, information processing occurs in neurons; each neuron is a small single processor whose response is non-linear. Individual neurons are able to perform very simple tasks which are further transferred to other neurons by connection links. These connection links have an associated weight and this weight multiplies as the signal is transmitted between different neurons [1, 5, 6].

Besides, the architecture of an ANN is a pattern of connections between the neurons; training or learning methods determine the connections' weights, and their activation function, which is a function of the input values it has received. Usually, a neuron sends an activation function as a signal to many other neurons. Although it can send only one signal at a time, that signal is broadcasted to several neurons. Some of the activation functions of ANNs are: identity, binary or unit step, piecewise linear, sigmoid, Gaussian and sinusoidal, among others. One, two, or more layers can constitute an ANN. Also, it has input (Xi) and output connections (Y). Inputs can be analog or digital signals. Synaptic weights (Wj) (also called gain or strength) are values associated with a connection path between two processing elements in an ANN and activation function f(x) is a function (mathematical equation) that transforms the net input neuron into its activation (Fig. 12.2), also known as a transfer function or output.

Output propagations can be backward or forward [7-13].

Inverters, designed and interconnected in the proposed circuit, generate at its output a Gaussian-type wave form. To improve the function, an alternative circuit was proposed with an inverter and an operational amplifier, which improves its Gaussian-type output function. With the purpose to verify the correct operation of n-type and p-type FGMOS transistors, it is important to first make measurements, so current-voltage characteristics (I-V), and transconductance behaviors of real FGMOS transistors were performed and compared to previous simulation made with OrCAD. At the end, inverter measurements indicated there was an appropriate operation.

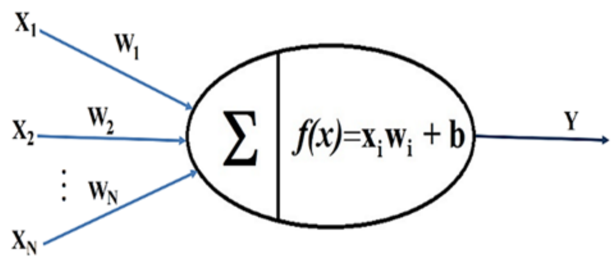


**Fig. 12.2.** ANN diagram.

## 12.2. Development

### 12.2.1. USB 6009 Data Acquisition Device by NI

An electronic circuit using op-amps was designed for signal conditioning; a non-inverting voltage follower op-amp was used, because it has high input impedance and supplies adequate current values to a data acquisition system. Also an electronic system was developed for data acquisition. This system used a USB 6009 data acquisition device by NI. This data acquisition device can read output voltage of the prototype without producing electrical interference in the prototype performance, thus a huge electrical charge can avoid tiny dimensions' inverters.

The first measurements had problems because of inherent electronic noise in the board. Fig. 12.3 shows a plot of the noise delivered by the electronic board; a filter was implemented to reduce this noise, and the signal after filtering is shown in Fig. 12.4 [14, 15].

A Gaussian function was desired for a perceptron ANN architecture, therefore, a circuit was designed by using both n-type and p-type FGMOS transistors. The designed electronic schematic circuit is shown in Fig. 12.5.

As it can be seen here, each transistor has its own floating gate, so adjustment of charge is made separately for each transistor. This gives the opportunity to reliably achieve the target function. The designed coupling coefficient value for either the n-type or the p-type FGMOS transistors was $K_{cg}$ = 0.28. An equivalent circuit has tree inverters INV1, INV2 and INV3, an input signal VG1 and an output signal VOUT. VG1 is joined to both INV1 and INV2 inputs; INV1 and INV3 are joined in cascade, and INV3 output is joined to P4 gate; INV2 output is joined to N4 gate (Fig. 12.6) [7, 9, 13].

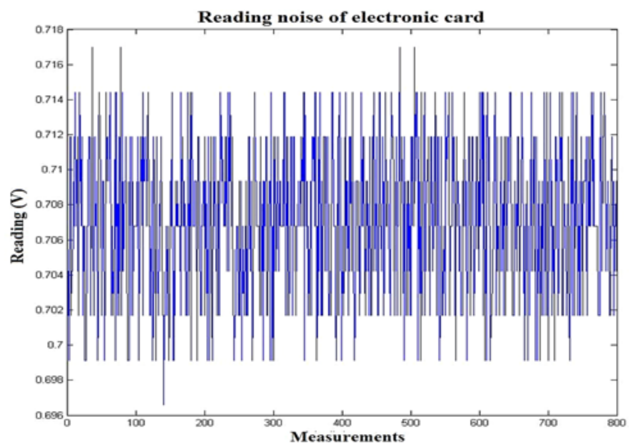


**Fig. 12.3.** Reading noise.

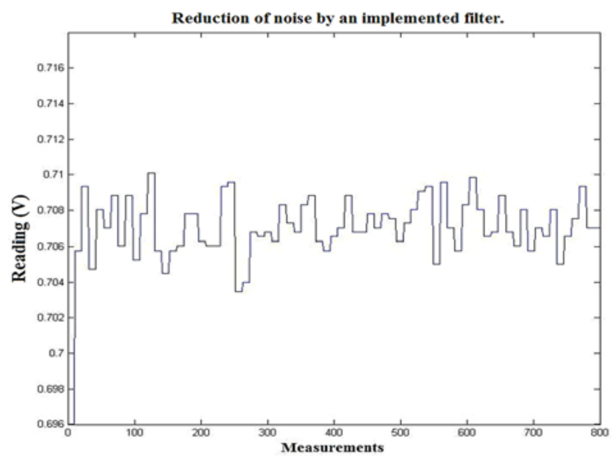


**Fig. 12.4.** Reduced noise measurement.

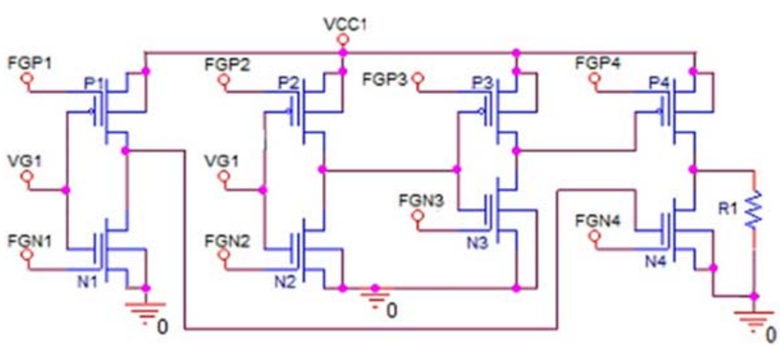


**Fig. 12.5.** An electronic schematic circuit for a Gaussian function (ANN).

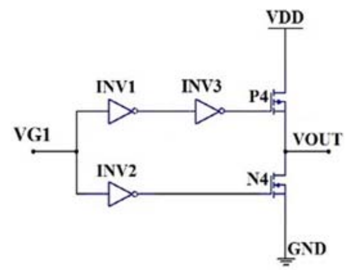


**Fig. 12.6.** An equivalent electronic circuit for a Gaussian function (ANN).

After several simulations made regarding the mentioned inverters, the capacitance that can best fit with the trade-off purposes of inverter's performance and design area was 0.1 pF. FGMOS transistors were designed by using 0.5 AMIS technology. Hence, the defined dimensions for the capacitance control gate that resulted from simulations and design rules for this technology were $37\lambda \times 37\lambda$, where $\lambda = 0.3$ μm. Starting from the technological data, a 103 fF capacitance was obtained, while the transistors dimensions were as follows: $W_n = W_p = 6\lambda$, $L_n = 4\lambda$, $L_p = 2\lambda$.

The circuit shown in Fig. 12.6 has some voltage variations due to a double inverting effect. So, alternatively, another circuit was proposed that has better performance characteristics. Furthermore, this alternative circuit eliminates undesired issues that are present in the former circuit, at the expense of introducing an operational amplifier and its corresponding external resistances. The proposed alternative circuit is shown in Fig. 12.7 and the Equivalent alternative circuit in Fig. 12.8 (op-amp).

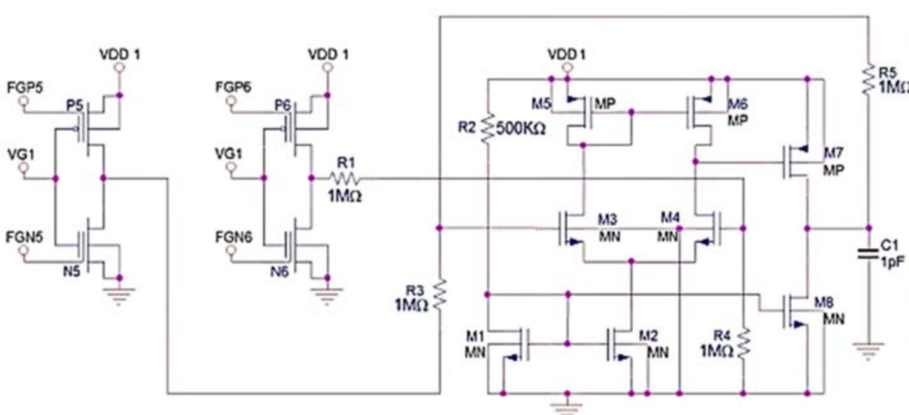


**Fig. 12.7.** Alternative circuit (op-amp).

In order to verify the correct operation of all modules and circuits, this ASIC circuit was tested through the data acquisition board mentioned above, with which it is possible to computationally interact with the circuit, giving the possibility to know the behavior of the proposed model and validate it. The test consists in applying an input ramp voltage to the gate of a FGMOS transistor. A series resistor is used to limit the current flowing through the transistor, and also to determine the current that flows through the transistor, making possible to obtain transconductance curves that define the transistors.

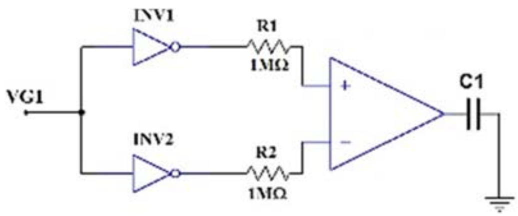


**Fig. 12.8.** Equivalent alternative circuit (op-amp).

Figs. 12.9 and 12.10 show plots of both, the input voltage and the output voltage as a function of time, with different magnitudes of charge present over the floating gate of the FGMOS, with $V_{DD}$ = 5 V. In Fig. 12.9 It should be noted that the circuit output plot is similar to a narrow Gaussian shaped function. The output function can be expanded or inverted as desired thanks to the FGMOS. Moreover, a negative function can be generated also as is shown in Fig. 12.10. This may be useful if one remembers that neurons can be excited with positive or negative inputs.

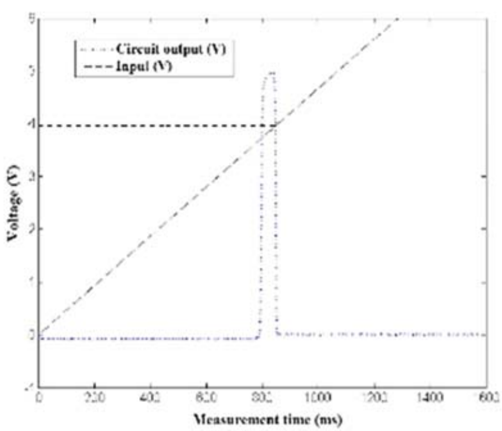


**Fig. 12.9.** Narrow pseudo Gaussian function of the circuit shown in Fig. 12.8, with an input ramp voltage.

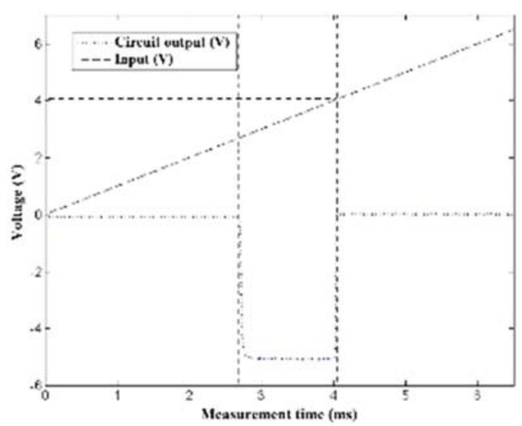


**Fig. 12.10.** Inverted output due to the modification of voltage values that represent the charge of FGMOS transistors.

## 12.3. Tests Performed to the FGMOS Transistors of the Prototype

The tests performed to the FGMOS transistors allow knowing whether there is a charge in the floating gate or not, making possible to set the transistor to a neutral or any defined charge in order to characterize its operation.

This is very useful since it allows to establish the programming procedure, for injection of charge into the floating gate of the FGMOS transistors, which leads to the consecution of the pseudo Gaussian function. Fig. 12.11 shows the output I-V curve of an n-type FGMOS presenting a charge in the floating gate which goes against the transistor's polarization. That is noticeable because $I_{ds}$ is near 0 A when $V_{gs} < 1.5$ V. Therefore, the voltage $V_{gs}$ must be higher than 1.5 V to form the transistor's channel. It is worth noting that the threshold voltage for these transistors and for this technology is $V_{th} = 0.67$ V.

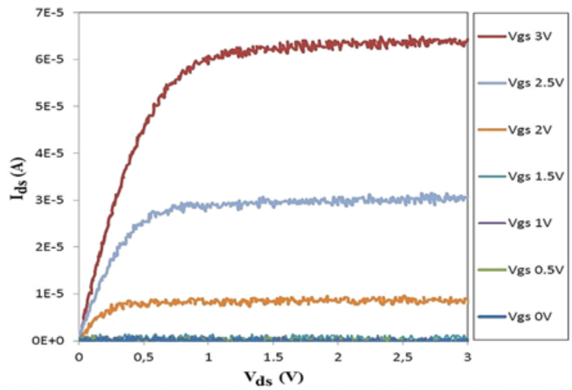


**Fig. 12.11.** N-type FGMOS characteristic plot (AMIS 0.5 technology).

It is commonly known that transconductance is a figure of merit for every MOSFET. In this case, an n-type FGMOS transconductance plot is shown in Fig. 12.12. Besides, for the designed coupling coefficient, the apparent threshold voltage, $V_{th}$*, must be approximately 2.45 V when there is not residual charge over the floating gate. $V_{th}$* is the threshold voltage of a FGMOS when $I_{ds}$ is plotted as a function of the control gate, $V_{gs}$, not the floating gate, $V_{fg}$ ($V_{th}$(N-MOS) = 0.82 V). Hence, any deviation from this value is indication of the presence of charge upon the floating gate. If the transconductance plot is shifted to the right, there is extra negative charge on the floating gate and when shifted to the left, positive charge is present. Regarding Fig. 12.12, it can be seen that there is no charge present on the floating gate since the apparent threshold voltage for this FGMOS is approximately 2.45 V.

On the other hand, Fig. 12.13 shows the output curve of a p-type FGMOS. In this case it can be seen that even when $V_{gs} = 0$ V, a current already flows across the FGMOS due to the presence of a negative charge; the typical threshold voltage for FGMOS is $V_{th} = -0.86$ V and the apparent threshold voltage, for this p-type FGMOS should be approximately Vth* = -2.4 V (Vth(P-MOS) = -0.92 V).

Next, Fig. 12.14 shows a p-type FGMOS transconductance curve, so it can be appreciated that a current is already present even for positive voltages, which means that the floating gate has a charge that promotes by itself the channel formation of the p-type FGMOS transistor even with when $V_{gs} = +0.5$ V.

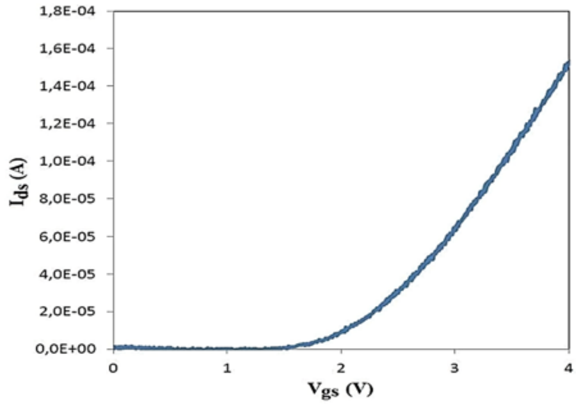


**Fig. 12.12.** N-type FGMOS transconductance plot.

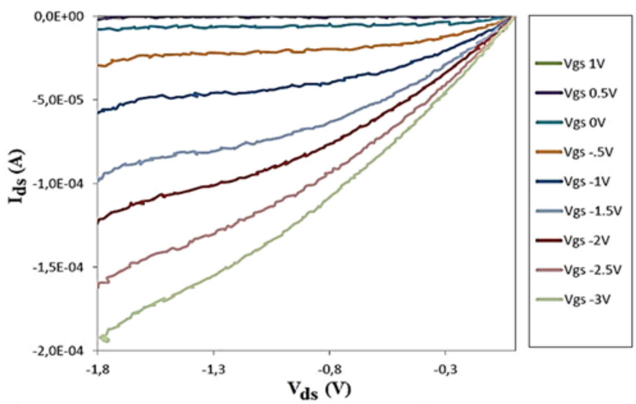


**Fig. 12.13.** P-type FGMOS characteristic plot (AMIS 0.5 technology).

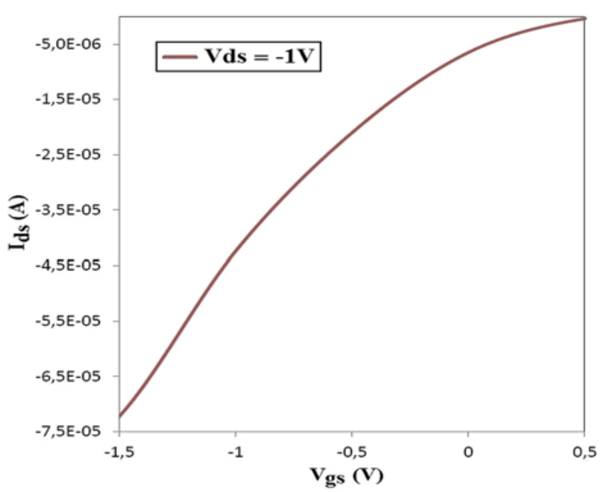


**Fig. 12.14.** P-type FGMOS transconductance plot.

Besides, the validation of the FGMOS transistor model is necessary in order to determine whether simulations fit closely to experimental data. For this reason, a comparison was made between the plots relating the experimental results of the prototype transistors and the simulations carried out using OrCAD® simulation software. Every simulation was carried out under the same polarization characteristics, this is, same voltage and same probe inputs. In the case of the n-type FGMOS transistor, it should be mentioned that a negative charge polarity inhibits the inversion channel to be present at control gate voltage values above the typical threshold voltage. The same will occur when positive charge is present on the floating gate of p-type FGMOS transistors.

Other comparisons between developed models used in a simulation program and the experimental measurements of the prototype transistors were made. In most cases, behaviors have very similar performances. This can be seen in Figs. 12.15 and 12.16 for the output and transconductance I-V characteristics, respectively of a n-type FGMOS. Also this comparison is made in Figs. 12.17 and 12.18 for the output and transconductance I-V characteristic, respectively of a p-type FGMOS. It can be seen that in all cases there is a good approximation between simulated curves compared with experimental data.

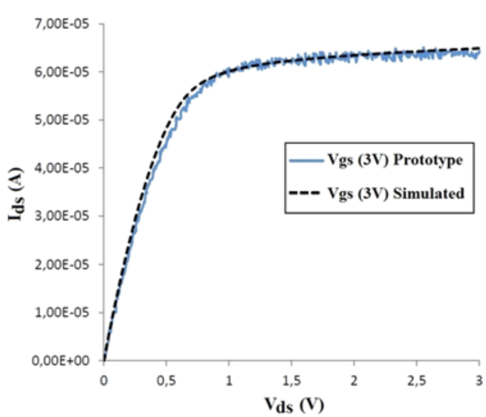


**Fig. 12.15.** Characteristic plot of both simulation and prototype n-type FGMOS transistors, for $V_{gs} = 3\,V$.

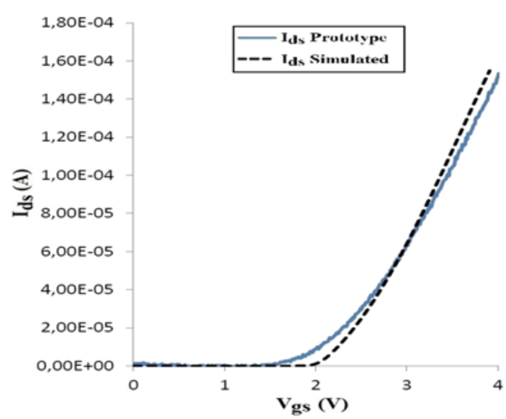


**Fig. 12.16.** Transconductance plots of both simulation and prototype of n-type FGMOS transistors, for $V_{gs} = 3\,V$.

### 12.3.1. Charge Inside Floating Gate

It should be mentioned that depending the magnitude or the polarity, the charge can promote or inhibit the formation of the channel in the transistor, even for positive or negative voltages applied to the control gate. For instance, Fig. 12.18 shows the transconductance characteristic curve of a p-type FGMOS transistor with voltage Vds = -1 V.

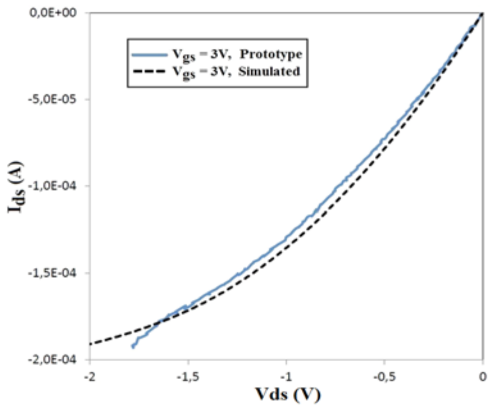


**Fig. 12.17.** Characteristic plot of both simulation and prototype n-type FGMOS transistors, for $V_{gs} = 3$ V.

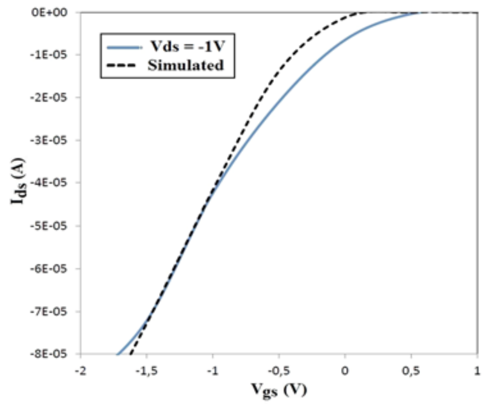


**Fig. 12.18.** Simulation and prototype transconductance plots of a p-type FGMOS transistor, Vds = -1 V applied.

Furthermore, it shows that the results of the simulated model and the experimental measurement are very approximate. The apparent measured threshold voltage for this p-type FGMOS is approximately $V_{th}^* = -0.3$ V. Since the expected apparent threshold voltage in a neutral FGMOS is $V_{th}^* = -2.4$ V, this right-shifted curve indicates the presence of negative charge that enhances the presence of a conductive channel between drain and source, even with negative voltages lower than this last voltage, applied to the control gate. Then, this is a demonstration that if charge can be injected or extracted to or from the floating gate, this can be used to modulate the electrical performance of the FGMOS, such that it can be used as a variable input weight within a learning algorithm in a supervised ANN. Injection/extraction of charge can be made by means of Fowler-Nordheim tunneling, and this is the method used in this work to program off-line both types of FGMOS transistors, in order to achieve the desired pseudo-Gaussian function to accomplish the correlation of gas species with a readable electric signal, as is proposed in this work.

Some experiments on this issue were tried and the results are shown next.

### 12.3.2. Final Tests

Several tests were carried out to transistors that are part of the ASIC prototype. Tests have demonstrated the possible modification of the behavior of an inverter formed by floating gate transistors. The results are shown in Figs. 12.19 to 12.22. The initial test of the inverter is shown in Fig. 12.19, where the output of the ANN shown in Fig. 12.8 was measured when a signal was applied to the input of the ANN, with these characteristics: first, a growing ramp with a slew rate of 3 V/1.33 s, next, a fixed value of 3 V during 0.66 s, and finally, a decreasing ramp with a negative slew rate of 3 V/1.33 s. Here it can be seen that the expected inversion is present but does the normal rail to rail output voltage (0 to 5 V) is not obtained; after that, a pulse of 15 V was applied at 1 ms.

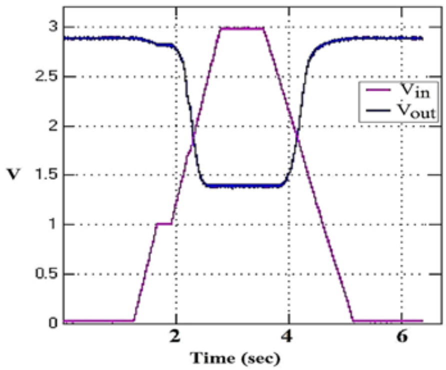


**Fig. 12.19.** Initial test of an inverter.

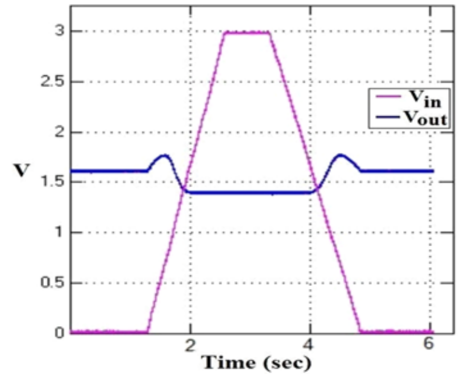


**Fig. 12.20.** Inverter response for 1 ms pulse of 15 V applied to n-type FGMOS transistor.

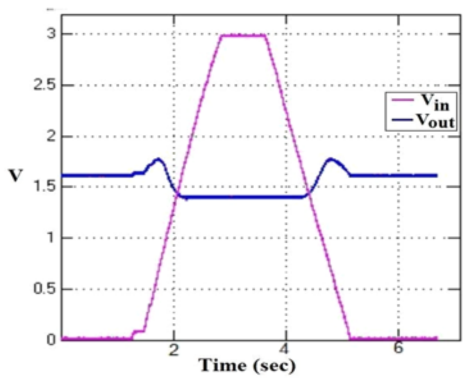


**Fig. 12.21.** Inverter response for three 1 ms pulses of 15 V applied to n-type FGMOS transistor.

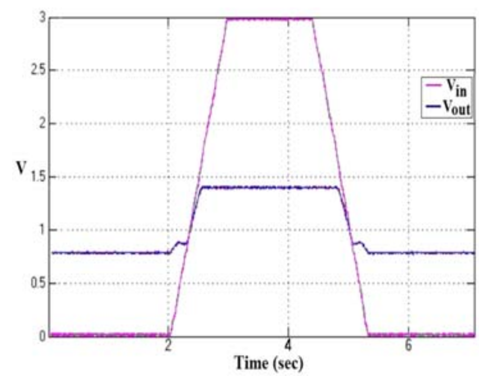


**Fig. 12.22.** Inverter's behavior after applying a pulse of 1 ms and -14 V applied to the floating gate of the p-type FGMOS transistor.

Fig. 12.20 shows the behavior of the inverter after programming the floating gate of n-type transistor. It is observed that the inversion is now more limited in terms of voltage values; because of this unwanted result, such charge in the n-type transistor gets deprogrammed.

The results of applying the test input after a series of pulses of -15 V for 1 ms are shown in Fig. 12.21. In this case, behavior variations are not appreciated. It is presumed that bigger voltages are required when it is wanted to decrease the charge in the floating gate. It is assumed that this behavior is due to charge extraction process that is carried out in the bottom side of the silicon oxide layer between polysilicon 1 and polysilicon 2, while charge injection process is carried out in the top layer of the oxide. It can be presumed that the surface is different in both sides. Due to its defects, the electrons traverse the superior surface easier than the inferior surface. That results in a substantial increase of charge extraction voltage. In order not to damage the n-type transistor with voltages higher than 15 V, the process was suspended. P-type FGMOS transistor was programmed by applying -14 V for 1 ms to the floating gate. The results are shown in Fig. 12.22. Now, the inverter has a behavior similar to a voltage follower because charges were injected in n-type and p-type gates of the transistors.

Two mechanisms are normally used to inject (extract) charge to (from) the floating gate: (a) hot electron injection and (b) carrier tunneling. Both of them are based on the electric field established between proper terminals of the devices.

## 12.4. Layout

The layout design for the development of an integrated circuit defines the elements that are going to be part of the Application Specific Integrated Circuit (ASIC), as well as the connections between them and the different structures and techniques, that allow eliminating the external noise and also defining the connections towards the package pins. Fig. 12.23 shows the whole design of an IC for AMIS 0.5 technology.

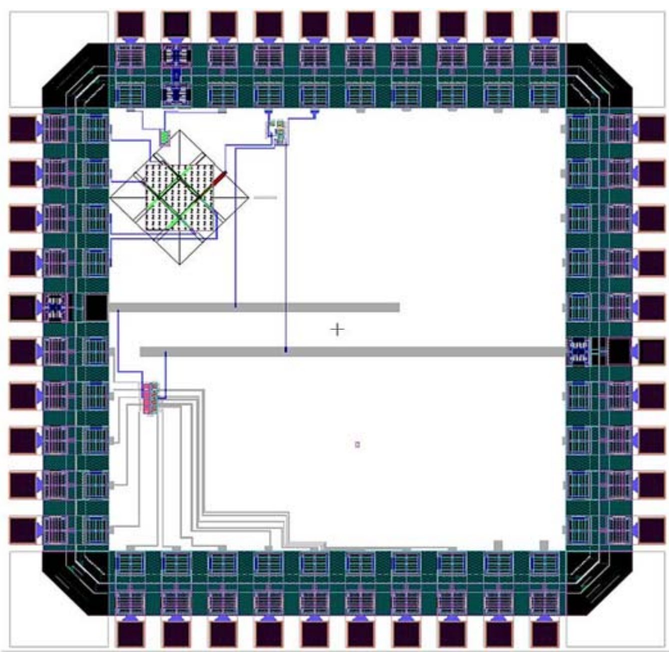

**Fig. 12.23.** Layout of the integrated circuit.

The circuit proposed to generate the Gaussian function is shown in Fig. 12.24. It is formed by four inverters, which, working together, allow generating the Gaussian function by modifying the charges in the FGMOS floating gate. The alternative circuit layout and the op-amp are shown in Fig. 12.25. The design also includes guard rings that prevent and avoid noise from the environment and another undesirable effects. On the other hand, structures that prevent charges in the floating gates during fabrication their fabrication, were added.

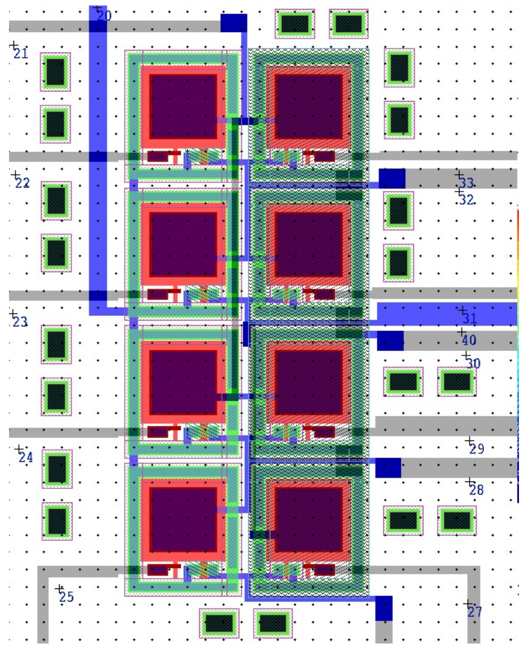


**Fig. 12.24.** Layout of the circuit proposed to obtain the Gaussian function.

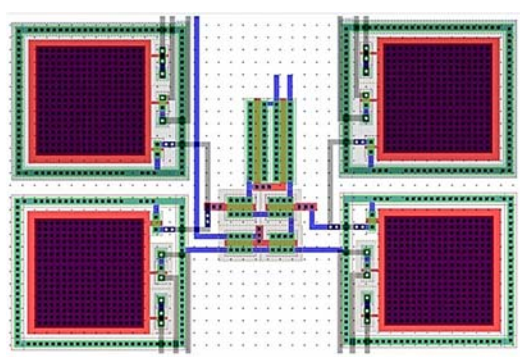

**Fig. 12.25.** Layout of the alternative circuit for Gaussian function (op-amp).

## 12.5. Conclusions

The dimensions of the lengths (L) and widths (W) of the channels are Wn = Wp = 6λ, Ln = 4λ, Lp = 2λ. The transistors' simulation was performed with Orcad®. After that, inverters for the circuit of ANN Perceptron were implemented. Several tests on current and voltage (IV) and on transconductance were carried out, which are essential to guarantee proper operation. An alternative circuit was designed with an inverter and an op-amp using n-type and p-type FGMOS transistors. Such circuit provides a Gaussian-type signal of positive and negative values. An electronic data acquisition card was developed to characterize the designed circuits, and an interface based on Simulink in

Matlab® was used to read data provided by the integrated circuit. During test procedure, different voltage levels were applied to floating gates of FGMOS transistors to verify the exchange of charges inside the gates. The transistors' gates are charged since their fabrication, therefore the threshold voltage was modified and signal's inversion was not performed. It was noticed a change in the FGMOS transistor's response when a positive voltage pulse of 15 V was applied to n-type FGMOS transistor. This means that both negative charges and the threshold voltage were increased. After that, -15 V were applied to the same floating gate of n-type FGMOS transistor. Although there was no reversion process, it is assumed that the negative voltage that is necessary to decrease the charge is higher than the applied voltage when such charge was increased. After that, -14 V were applied to the floating gate of p-type FGMOS transistor, making the circuit to behave as a follower.

At the end, an integrated circuit was designed and produced using the 0.5 μm AMIS technology. The integrated circuit contains the proposed and alternative circuits for a perceptron ANN. This integrated circuit will serve as a basis for its future integration to a gas sensing system.

## Acknowledgements

The authors want to thank to M. Sc. Luis Martín Flores Nava for his grateful support in the circuit design, simulation and characterization.

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