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TECHNICAL PAPER

Inertial sensing MEMS device using a floating-gate MOS transistor as transducer by means of modifying the capacitance associated to the floating gate

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Abstract
In this work, a novel application of floating gate MOS transistors is presented. An inertial sensor with an embedded FGMOS was designed, simulated and fabricated using commercially available CMOS technology, like the ON Semiconductor 0.5 μm, two poly, three metal, N-well, post-processed using a surface micromachining etchant to obtain a CMOS-MEMS chip, and tested. COMSOL multiphysics was used for electro-mechanical evaluation of the inertial system, PSPICE for electrical behavior analysis, Keithley instruments for electrical characterization, and Labview for data acquisition for electrical characterization. In this work, it is demonstrated that an embedded FGMOS can be used to correlate drain current either for static or dynamic inertial parameters. The presented work demonstrates the feasibility to change the coupling coefficient of the FGMOS by means of a MEMS structure, like an accelerometer, to convert displacement into an electrical signal, being suitable for integration in more complex systems.

1 Introduction

The floating gate MOS transistor (FGMOS) is a device mainly used in non-volatile flash memories (Hasler et al. 1999), but also it can even be used in its volatile configuration in several digital and analog circuits such as op-amps (Jamal et al. 2011), comparators (Rodriguez-Villegas 2005), or current mirrors (Gupta et al. 2014; Singh and Kumar 2016), that have been reported taking advantage of the operating feature given by the floating gate of this device. In (Mourabit et al. 2004) the FGMOS is also used within the design of an OTA amplifier and in Hang et al. (2014) and Gopal et al. (2015) the FGMOS is used to perform binary and ternary logic, respectively. These are a few examples of the wide field where the FGMOS have found toward digital and analog applications with CMOS integrated circuits. However, the goal in this work is to show that the operation of the FGMOS can be taken further beyond the already known circuit applications, i.e. in CMOS-MEMS, establishing a variable coupling coefficient

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through a coupling capacitor actuated mechanically, which is connected between the control gate and the floating gate of a FGMOS transistor. This monolithic approach, consisting in having the CMOS circuitry and the MEMS structure in the same substrate (Baltes et al. 2002), reduces the setbacks associated with the hybrid integration of electromechanical devices and the corresponding signal conditioning circuits (Brand 2005).

Some examples of similar developments in which MEMS and CMOS technology are combined to form an inertial sensor are shown in Yee et al. (2000) and Aoyagi et al. (2011). In Yee et al. (2000) an integrated accelerometer is shown, unlike the one presented in this work, an oscillator element is required for its correct functioning. In Aoyagi et al. (2011) the inertial sensor requires altering the structural material in order to achieve enough sensitivity. It is important to emphasize that the main goal of this work is to demonstrate the use of a floating gate sensor coupled with an inertial capacitive sensor and to demonstrate that its use is feasible in inertial sensors. However, the CMOS-MEMS route is limited by the design constrictions determined by the selected CMOS technology, especially the available structural and sacrificial materials, thickness, number of layers, size restrictions and so forth.

In the presented work, these factors are taken into account to develop an inertial sensor with an active electronic device integrated in the mechanical structure. This represents a novel way to use the FGMOS that has not been reported before by other authors, using this device as an electromechanical transducer instead.

2 The FGMOS as an electromechanical transducer

A floating gate MOS transistor, as the name implies, is a MOSFET with the gate electrically isolated, with no resistive connections to this terminal, converting it in a floating node; instead, the input or inputs, are only capacitively coupled to this isolated or floating gate (FG). Figure 1 shows the schematic for an n-channel, *n*-inputs FGMOS transistor showing the associated capacitances (Yee et al. 2000).

The voltage induced over the isolated gate of the transistor is known as the floating gate voltage (V_{FG}); this voltage depends on the voltages applied over the control gates, as well as in drain, source and bulk terminals, as is expressed in (1) for a FGMOS with more than one control gate (Aoyagi et al. 2011):

$$V_{FG} = \sum \alpha_{CGi} V_{CGi} + \frac{C_{GD}}{C_T} V_D + \frac{C_{GS}}{C_T} V_S + \frac{C_{GB}}{C_T} V_B + \frac{Q_{FG}}{C_T}, \tag{1}$$

where:

$$\alpha_{CGi} = \frac{C_{Gi}}{C_T}, \tag{2}$$

$$C_T = \sum_i C_{Gi} + C_{GD} + C_{GS} + C_{GB}, \tag{3}$$

where C_{Gi} is the capacitance due to each of the n control gates, V_{CGi} is the voltage applied to control gate i, C_T is the total equivalent capacitance, V_D is the drain voltage, V_S is the source voltage, V_B is the bulk voltage, C_{GD} is the parasitic capacitance between the drain and the floating gate, C_{GS} is the parasitic capacitance between the source and the floating gate, Q_{FG} is any residual charge that may be present on the floating gate, and α_{CG} is defined as the coupling coefficient and is always less than 1 (Rodriguez-Villegas 2006, 2007).

As it is well known, the capacitance value is inversely proportional to the distance between the plates separation, $C' = (\varepsilon_0 \varepsilon_r)/d$, where C' is capacitance per unit area, ε_0 is vacuum permittivity, ε_r is dielectric relative permittivity, and d is the distance between capacitor plates. Then, from (1) it is easy to see that any change in α_{CG} will be reflected as a change in the electrical behavior of the FGMOS through V_{FG}, although the control gate voltage is fixed. A thorough analysis of the electromechanical model of this device is presented in Abarca-Jiménez et al. (2015, 2016).

About the residual charge concern, six test FGMOS were included in the prototype integrated circuit with W = 20λ and L = 4λ (λ = 0.3 μm), but each with different size of coupling capacitors. The V_{th} of each FGMOS was measured as received from the foundry. It was found that floating gates had negative or positive random charge. For good operation of the proposed accelerometer, it is desirable not to have residual charge, so the chip was illuminated with ultra violet light (UV), until there is no change in the threshold voltage. This is an indication that this charge was completely removed. The result of this procedure is shown in Fig. 2, where it can be seen that after 120 s of UV exposure, charge was removed.

Having this in mind, one way to conceive a variable capacitance is by means of a finger comb array commonly used with MEMS accelerometers, which can measure acceleration or applied force, based for instance, in a differential capacitance array measuring the change in capacitance due to the mechanical movement, where demodulation has to be used in order to convert the

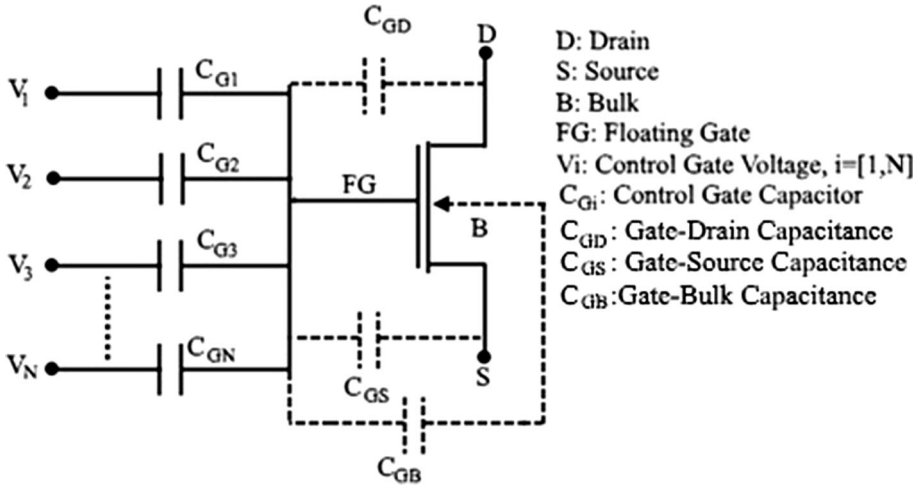

Fig. 1 Schematic representation of the associated capacitances of an n-channel, n-inputs, FGMOS transistor

measurement input signal into a dc output signal (Rodriguez-Villegas 2006) in a dynamical measurement, but also as an inclinometer for static measurements (Abarca-Jiménez et al. 2015, 2016). The proposal given in this work is a different and novel approach for inertial transduction.

The explanation of how a mechanically variable coupling coefficient can be reached is given next. A representation of the FGMOS as an electromechanical transducer is illustrated in the diagram shown in Fig. 3. The following elements can be identified: a proof or inertial mass, representing the inertial element, suspended by a spring whose anchor is one plate of the variable capacitance and is connected to the control gate of the transistor; on the other side, the other plate of this capacitance is fixed having the role of the floating gate of the FGMOS. Obviously, the dielectric of this capacitor is air. As was explained before, the FGMOS can operate with more than one control gate, but the configuration used in this work uses only one control gate. One extra control gate can be used so that the operation point of the transistor can be tuned with the help of the voltage applied to this extra control gate, remembering that the floating gate is a voltage summing node, whose magnitude can establish the operation regime of the MOS transistor. Hence, based in this mechanical structure, this device is a Floating Gate MOS transistor embedded in an electromechanical structure.

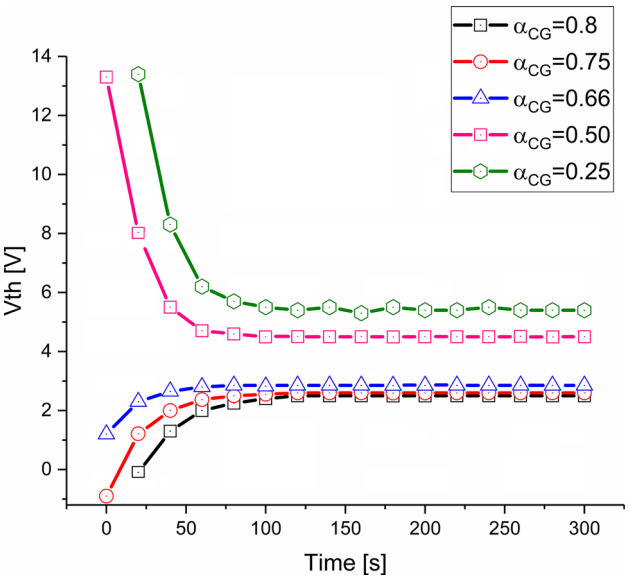

Fig. 2 Charge removed after 120 s of UV exposure

The drain current of the FGMOS can be related to tilt as follows. The inertial mass is supported by springs anchored to the fixed frame, with total spring constants k_x, k_y and k_z, corresponding to the axis of movement. By design, k_y and k_z are much larger than k_x, allowing only forces exerted over the x-axis to affect the inertial mass. When tilt angle (θ) is zero degrees, the force (W_m) over the inertial mass due to gravitational acceleration (g) has no x-axis component, so C_G has a value determined by the physical layout and the technological design rules. As the x-axis of the device is tilted, this capacitor will change its value because the plates will be closer or further apart, being this an effect of the x component of W_m, as shown in Fig. 4a, b.

Considering k_y, $k_z \ggg k_x$,

$$W_{mx} = W_m \sin(\theta), \tag{4}$$

which is the applied force on the spring, F_s:

$$F_s = -k_x \delta, \tag{5}$$

where δ is the spring displacement, hence, we have:

$$\delta = \frac{W_m \sin(\theta)}{k_x}. \tag{6}$$

Thus, the expression for the parallel plate capacitors formed by a moving electrode and a fixed electrode (Rodriguez-Villegas 2006) in this device, yield the next equations considering that the control gate capacitor

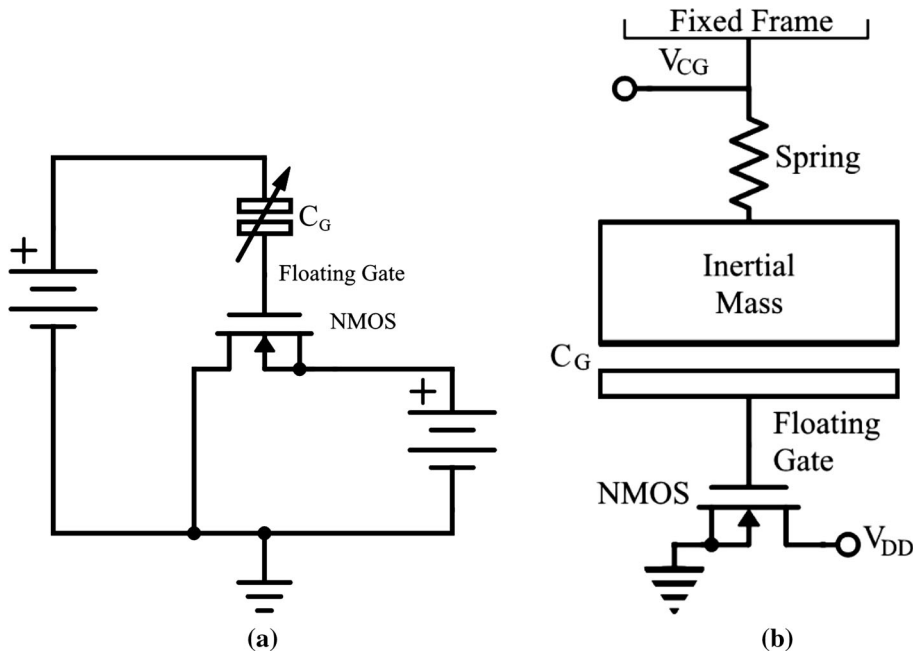

Fig. 3 **a** Schematic diagram of a FGMOS with variable coupling coefficient; **b** equivalent electromechanical diagram, where V_{CG} is the control gate voltage

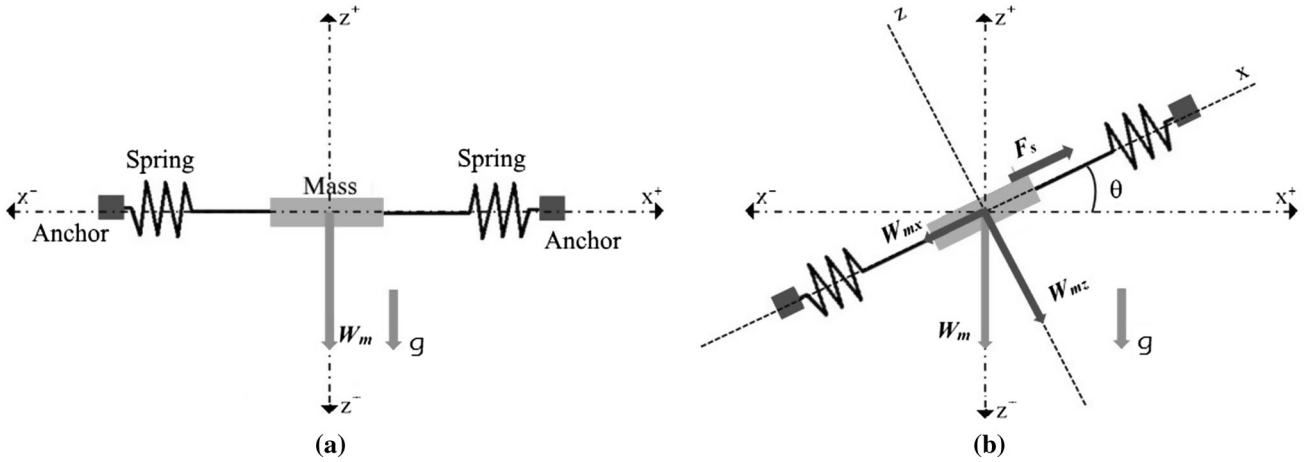

Fig. 4 **a** Mechanical structure at 0° tilt; **b** tilted structure, showing components of applied force

consists of an arrangement of parallel capacitors, with two distinctive components (see Fig. 5):

$$C_{11} = \varepsilon_0 \varepsilon_r \frac{A}{d_1 + \delta}, \tag{7}$$

$$C_{22} = \varepsilon_0 \varepsilon_r \frac{A}{d_2 - \delta}, \tag{8}$$

where d_1 and d_2 are the separation between plates of the respective component capacitor, ε_0 the vacuum permittivity, ε_r the insulator permittivity, air for the presented device, and A the overlap area. These expressions constitute the variable parts of the control gate capacitor (C_G) of the device. Finally, the control gate capacitor is, then

$$C_G = N(C_{11} + C_{22}). \tag{9}$$

Being N is the number of moving-fixed electrode pairs of C_{11} and C_{22}, where both will change when a force is applied along the x-axis (Rodriguez-Villegas 2006). For instance, when a force is applied along the positive x-axis direction, C_{11} will be larger than C_{22} since d_1 turns smaller than d_2, so their initial value when $\theta = 0°$ is different, as can be seen in Fig. 6.

As the device is tilted further, for example toward positive angles, C_{22} grows larger since d_2 decreases and on the other side, C_{11} reduces because d_1 now increases. This is shown in Fig. 6a. Equation (9) describes the behavior of the control gate capacitor taking these considerations into

account and all the capacitor pairs that integrate the control gate, Fig. 6b illustrates this.

This last expression can be substituted in (1), (2) and (3), yielding an expression from where the voltage over the floating gate as a function of tilt angle can be obtained. This voltage is the effective voltage applied to the MOS structure, being equivalent to the gate voltage in a conventional MOSFET. Subsequently, in the variable depletion layer model (Abarca-Jiménez et al. 2015), V_{FG} can be used instead of V_{GS} in the drain current equation:

$$I_D = \frac{\mu_n C_{OX} W}{L}\left(V_{FG} - V_{FB} - 2\phi_F - \frac{V_{DS}}{2}\right)V_{DS} \cdots - \frac{2}{3}\mu_n \frac{W}{L}\sqrt{2\varepsilon_S q N_a}\left((2\phi_F + V_{DB})^{3/2} - (2\phi_F + V_{SB})^{3/2}\right), \quad (10)$$

where μ_n is the mobility, C_{OX} the gate oxide capacitance, W and L the drawn channel width and length of the MOSFET, respectively, V_{FB} the flat-band voltage, $2\phi_F$, the surface potential, V_{DS} the drain-source voltage, ε_s the semiconductor permittivity, q the electron charge, N_a the substrate impurity concentration, V_{DB} the drain-bulk voltage and V_{SB} the source-bulk voltage.

Therefore, considering all the above, Eq. (11) describes the behavior of the electromechanical structure, in which tilt angle affects the drain current, effectively acting as a transducer from a mechanical stimulus into an electrical signal:

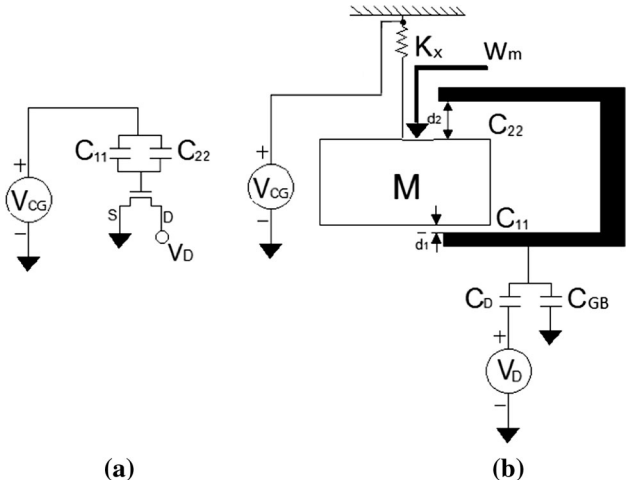

Fig. 5 **a** Electrical diagram for the inertial sensor; **b** electromechanical diagram for inertial sensor

poly, three metals) technology. Figure 7a shows the results for the I–V output plot for six different FGMOS designed with the mentioned coupling coefficients, and Fig. 7b is a plot of V_{FG} vs α_{CG}, and it can be seen that the result is according Eq. (1), since V_{FG} will decrease as α_{CG} decreases.

Values obtained from simulation and used for this plot, are shown in Table 1. The coupling coefficient was calculated using the ratio C_G/C_{TOT} derived from each of the six FGMOS considered. As it can be seen, the coupling

$$I_D = \frac{\mu_n C_{OX} W}{L}\left(\left(\frac{\frac{N\varepsilon_0\varepsilon_r k_x A}{W_m \sin(\theta)}\left(\frac{1}{d_1+1}+\frac{1}{d_2-1}\right)V_{CG} + C_{GD}V_D + C_{GS}Vs + C_{GB}V_B + Q_{FG}}{\frac{N\varepsilon_0\varepsilon_r k_x A}{W_m \sin(\theta)}\left(\frac{1}{d_1+1}+\frac{1}{d_2-1}\right) + C_{GD} + C_{GS} + C_{GB}}\right) - V_{FB} - 2\phi_F - \frac{V_{DS}}{2}\right)V_{DS} \cdots - \frac{2}{3}\mu_n \frac{W}{L}\sqrt{2\varepsilon_S q N_a}\left((2\phi_F + V_{DB})^{3/2} - (2\phi_F + V_{SB})^{3/2}\right) \quad (11)$$

3 Simulation of the FGMOS with a variable coupling coefficient

After several simulation tests with PSPICE, a MOS transistor with $W = 6$ μm and $L = 1.2$ μm was used to run a test in order to obtain the I–V output characteristic of the FGMOS transistor with different and arbitrary coupling coefficients. Figure 7 shows the result using the following set for α_{CG}: 1/4, 1/3, 1/2, 2/3, 3/4 and 4/5. The FGMOS simulated has only one control gate and the fixed voltage applied to this control gate (V_{CG}) was 5 V; a voltage sweep was applied to V_{DS} from 0 V to 3 V; $V_B = 0$ V.

The technological parameters used in this case correspond to ON Semiconductor's 0.5 μm (N-well, double coefficients are very close to the ones proposed.

It can be seen from this result that drain current for this transistor with $V_{DS} = 3$ V, goes from approximately 0.39 mA with $\alpha_{CG} = 1/4$, and up to 1.38 mA with $\alpha_{CG} = 4/5$ respectively, which are current magnitudes that can be easily handled with a simpler circuit to get an output signal correlating accordingly with an inertial input. It should be clear that the variable coupling coefficient is the result of an external applied force. This makes the proof mass to move such that the distance between the capacitor plates can be increased or decreased resulting in different capacitance according to the magnitude, direction of acceleration or force. Therefore, initially it is shown with this simulation that a FGMOS embedded in an

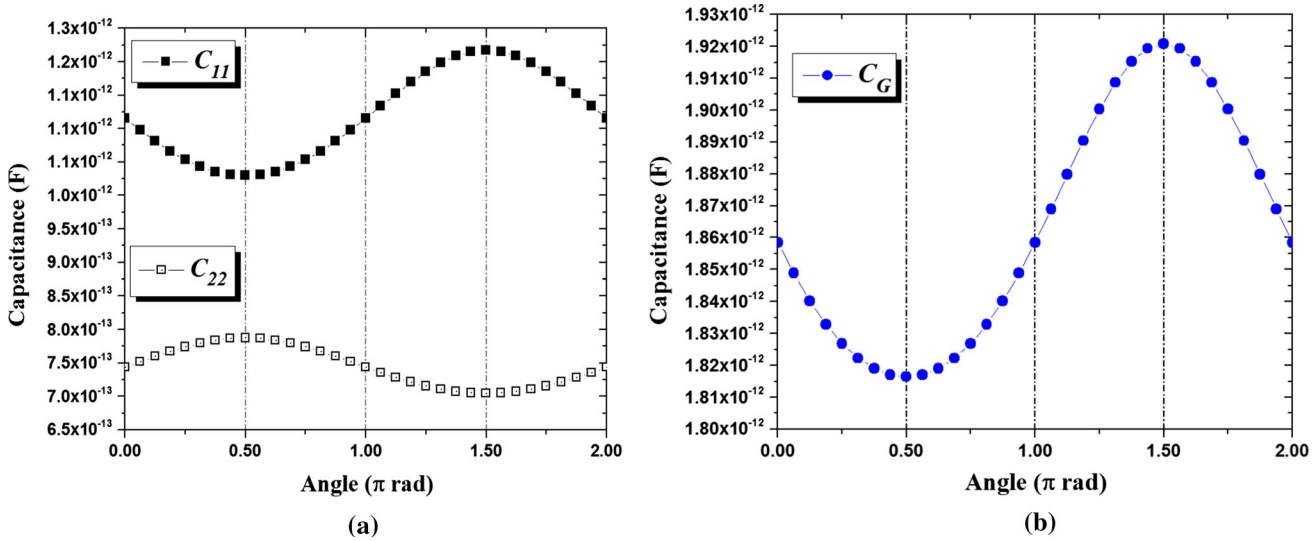

Fig. 6 **a** Behavior of the components C_{11} and C_{22} obtained from (7) and (8), respectively; **b** total behavior of C_G obtained from (9)

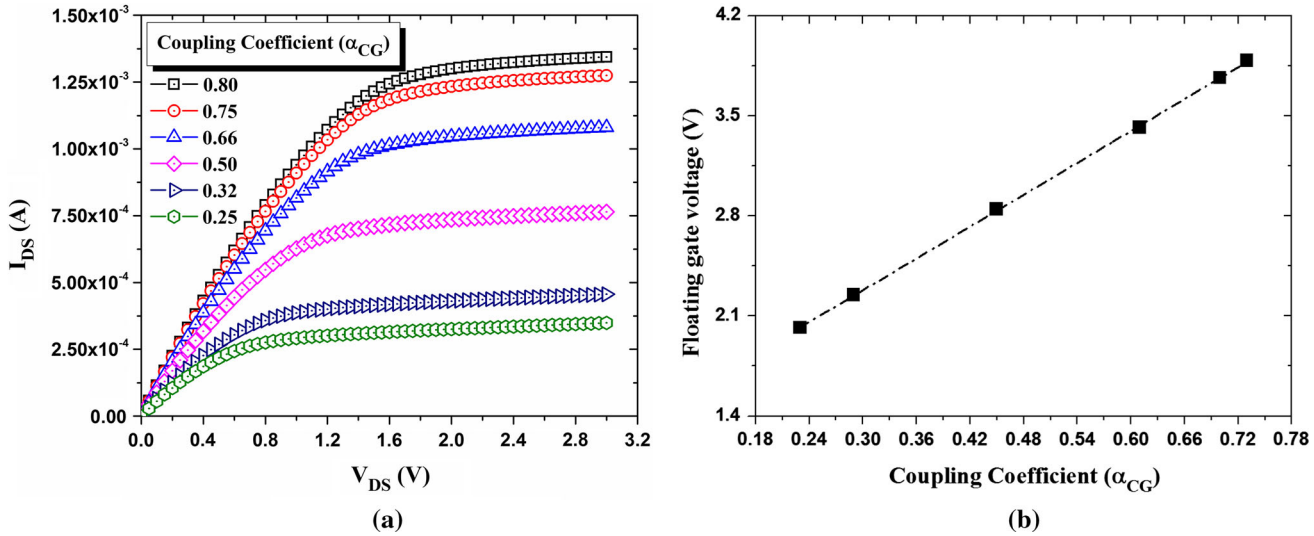

Fig. 7 **a** I–V output plot for a FGMOS with different coupling coefficients; **b** V_{FG} vs α_{CG}

electromechanical microstructure, like an accelerometer, can be used as an inertial transducer. The next sections explain the design, fabrication and test procedures that confirm experimentally the mentioned hypothesis.

4 Microstructure design for inertial sensing

The system was designed using ON Semiconductor 0.5 μm CMOS technology, which has two polysilicon layers and three aluminum layers for interconnection. The poly layers allow fabrication of FGMOS transistors, and the metal layers are used as structural layers for this electromechanical structure.

Table 1 Values obtained for α_{CG} and V_{FG} from SPICE simulation of an FGMOS

α_{CG}	V_{FG} @ $V_{DS} = 5$ V
0.73	3.8861
0.70	3.7642
0.61	3.4189
0.45	2.845
0.29	2.2456
0.23	2.0171

The design requires following the specific design rules of the selected technology, thus constraining the mechanical conception and evaluation of the inertial sensor, and also in the selection of the adequate sacrificial and

structural layers from the available layers of a particular technology and etchants used to release the structural layers.

For the case here reported, the structural layer of the fabricated device is made by stacking two aluminum layers (metal 1 and metal 2), using via plugs to mechanically join such layers. As the diagram in Fig. 3 shows, a plate of the control gate capacitor (C_G) is formed by the mass-spring system, whereas the other plate is formed by the opposing fingers in the corresponding fixed electrode, this is, the gate of the transistor. An interdigitated comb array of capacitors is built with the side walls of both pairs of comb electrodes, and since the whole electromechanical structure is intended to be micromachined to allow movement, the dielectric will be air. Figure 8 illustrates the configuration, showing in a simplified way the mass, the springs and the comb capacitor.

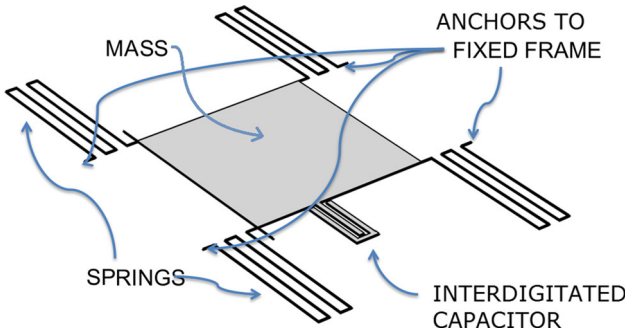

Fig. 8 Electromechanical configuration of the inertial structure

The layout of the mechanical structure and FGMOS transducers is shown in Fig. 9. As it can be seen, there are two FGMOS, each with $W = 6$ µm and $L = 1.2$ µm; both can be modeled from the electromechanical system shown in Fig. 3. At this point, it should be clarified that this work has only been tested using 0.5 µm technology; however, theoretically it can be applied to any other technology, as long as it complies with a series of requirements in order to determine the geometric aspect of the transistor:

- The effective area that can be used to place the capacitive structure.

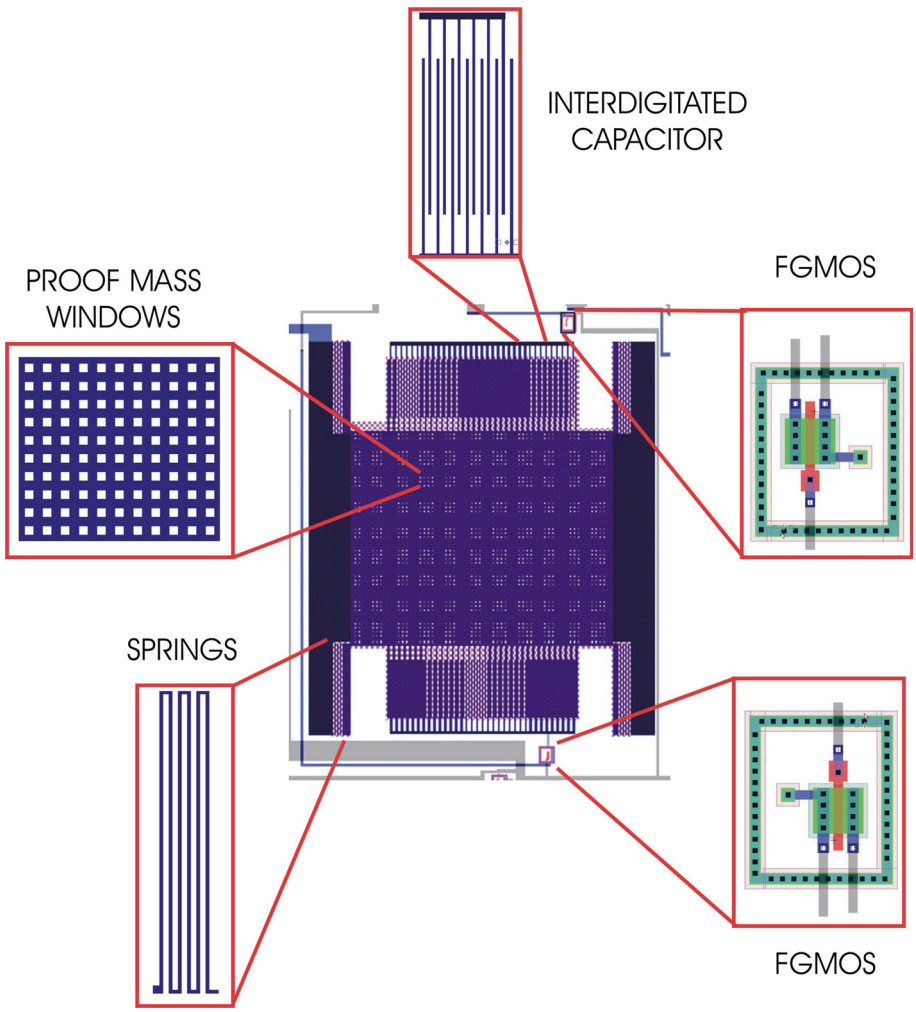

Fig. 9 Layout of the integrated system using ON Semiconductor 0.5 µm technology

- The target displacement of the moving mass, limited by two elements, what range of capacitance is produced and the size necessary to achieve the displacement. This feature is limited by the effective area that can be used.
- The range of capacitance of the structure is a function of two elements, the correspondence between acceleration–displacement–electrode distance, and the range of capacitance must be of the same order of magnitude as the total parasitic capacitance of the FGMOS all the time.
- Finally, the parasitic capacitance is in function of the size and shape of the transistor.

As it can be seen, if an arbitrary transistor size is selected, a specific capacitive structure must be designed for it. In another hand, if a capacitive structure is first designed, a transistor size must be selected from it. The rule to be followed is that the variation of capacitance must be of the same order of magnitude than the parasitic capacitance.

For our case, due to the extremely limited available area, a structure was designed that fits to this restriction and subsequently establishes the transistor size that delivers the appropriate parasitic capacitance and amount of current according to the measurement equipment.

In this case, one node is shared between the two FGMOS, where the control gate voltage (V_{CG}) is applied. It is important to note than that this node represents the voltage that sets the bias point for both circuits, but these can be treated independently. The intention of having two FGMOS is to identify the direction of movement in the sensing axis, since the separation between the plates of one capacitor will increase, while on the other side that separation will be decreased. If the direction of the applied force is inverted, the capacitors will have the reverse behavior. This behavior is shown in Fig. 10.

The capacitance variation is achieved as follows: the mechanical structure has a proof mass with a comb fingers array attached to it, held with springs, both made of a stack of aluminum layers anchored to the substrate. The opposite electrode is fixed all the time, so that the distance between the electrodes will change depending on the direction and magnitude of the inertial force applied in the proof mass. As a consequence of the relative movement of the proof mass, the control gate capacitor, C_G, will change and thus the coupling coefficient will change too, establishing a different operation point of the FGMOS. Therefore, the resulting shift in drain current can be related to the applied force. This way, a CMOS-MEMS inertial sensor is achieved, where the 3D electromechanical moving structure is integrated directly to electronic transducers in a monolithic substrate.

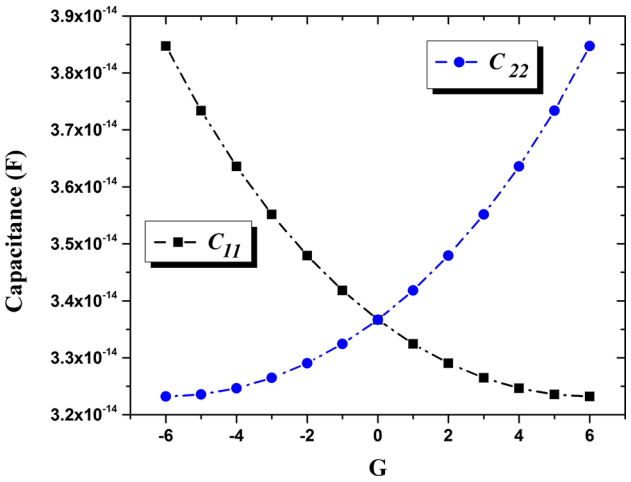

Fig. 10 Behavior of the control gate capacitance for both FGMOS included in the proposed design

As was mentioned in Sect. 2, the floating gate voltage depends on parasitic capacitance C_{GD}, C_{GS} and C_{GB}. These capacitances are included as part of total capacitance C_T, together with the channel capacitance, C_{OX}. The first three capacitances depend on the technology used and care must be taken in order to consider the values for the specific technology used in the accelerometer construction. Since lateral capacitance is fundamental for the comb array design of fingers of the accelerometer, metal layer thickness must also be considered, since each CMOS technology has its own values. It is important to take into account parasitic capacitances present on the FGMOS as they are part of the total capacitance C_{TOT} of the inertial system. A design strategy should be established to achieve a coupling coefficient (see Eq. 2) that can result in a feasible floating gate voltage, V_{FG}, that can drive the transistor into the desired operation point, i.e. saturation or sub threshold.

As it was specified before, ON Semiconductor's 0.5 µm technology was used since it offers two layers of polycrystalline silicon, from which FGMOS can be configured. This is a CMOS technology regularly used for CMOS integrated circuit design, in digital, analog or mixed signal circuits. Therefore, these technologies are not intended for fabrication of MEMS structures, although MEMS can be added to the layout following some design strategies that allow a micromachining process after reception (post-process) of the fabricated chip, as is shown ahead in this report. Of course, there are dedicated technologies for MEMS structure fabrication like PolyMUMPS and MetalMUMPS, but no peripheral electronic circuits can be included in the same chip.

5 Surface micromachining process

The 2 mm^2 chip (Tiny Chip) was fabricated by ON Semi, and delivered diced and wire bonded to a ceramic 40 pin Dual In-line Package (DIP40) with removable lid. Since the standard technological process for manufacturing the CMOS chip does not allow obtaining a released MEMS capacitive structure, a surface micromachining post-process is required. The micromachining of the structure was performed using Silox Vapox III from Transene®, directly filling the DIP40 cavity. This step etches away the exposed inter metal layer insulator (the sacrificial layer, IML, SiO_2), releasing the electromechanical structure, as this etchant preserves the aluminum layers (Kaajakari 2009). Then it was rinsed and oven dried, following the steps established in Table 2.

Figure 11 shows the bonded and packaged chip after surface micromachining, with no loose, deformed or otherwise damaged bonding wires.

Figure 12 shows an SEM photograph with the interdigitated capacitor (comb fingers), formed from the side walls of the aluminum fingers in the inertial mass (left) and in the frame (right). In the inertial mass, a series of openings through the aluminum layers can be seen. These orifices allow the etchant to completely penetrate below the inertial mass so it can be released. Next, a SEM image is shown in Fig. 13, where the behavior of a spring is evident because the chip was rotated 70 degrees from the horizontal. The etching of the IML can be clearly seen, along with the trace of the spring over the layer below due to a large warping of the spring. This effect was observed in only one sample, probably caused by a handling issue, as the structure had no damage from the micromachining. Nevertheless, this warping allowed for inspection of the micromachined surfaces below the metal stack.

The etching of the IML can be clearly seen, along with the trace of the spring over the layer below. Figure 14 shows several details of the interdigitated capacitor fingers. As described before, the structure is made stacking two aluminum layers, mechanically and electrically joined by via plugs.

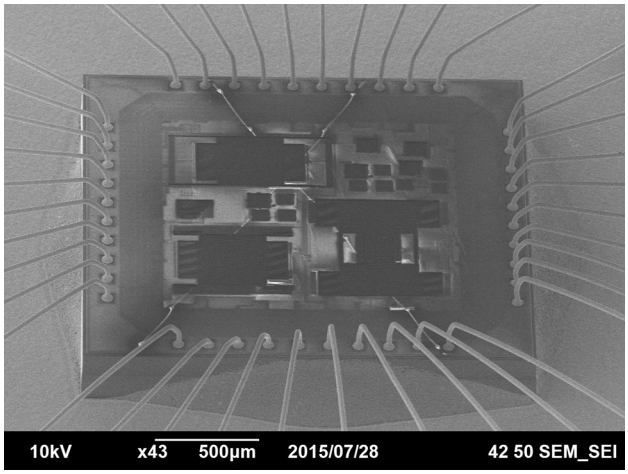

Fig. 11 Packaged chip after MEMS post-processing

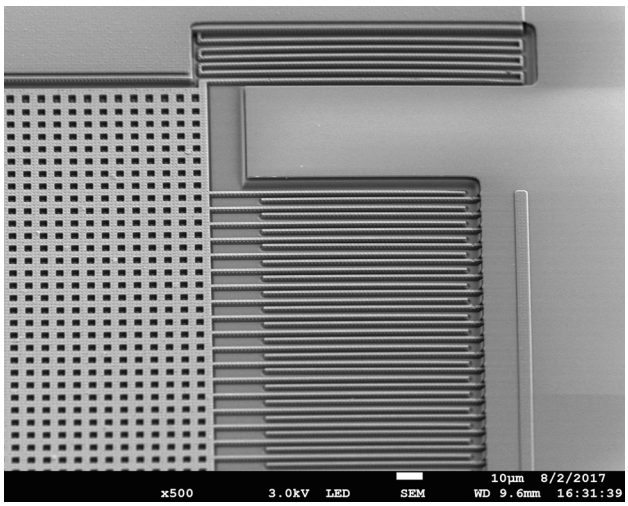

Fig. 12 The inertial mass (left) and the frame (right), forming the control gate capacitor (C_G)

6 Experimental results

The system was measured under static conditions at three different positions: first, with an angle of 0° with respect to the horizontal (0G, Fig. 15), second, with an angle of 90° (1G, Fig. 16), and third, with an angle of 270° (− 1G,

Table 2 Surface micromachining procedure with the encapsulated chip

Step	Procedure	Time (min)
1	Micromachining with Silox Vapox III, room temperature	15.5
2	Rinse with 25% isopropyl alcohol + 75% water	1
3	Rinse with 50% isopropyl alcohol + 50% water	1
4	Rinse with 75% isopropyl alcohol + 25% water	1
5	Rinse with isopropyl alcohol 100%	1
6	Dry in oven, 120 °C	40

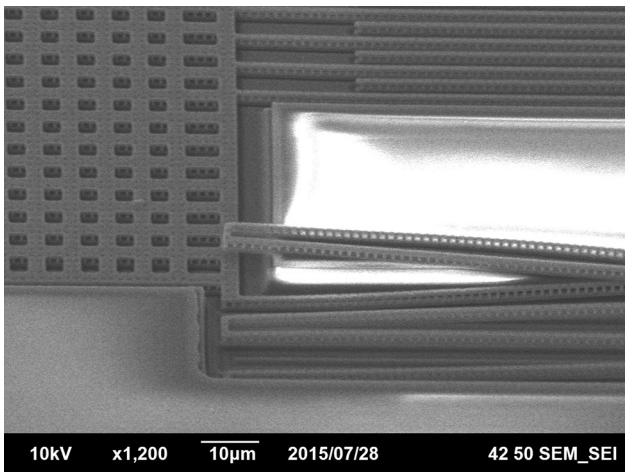

Fig. 13 Mass supported by the spring, with the SEM holding plate rotated 70°

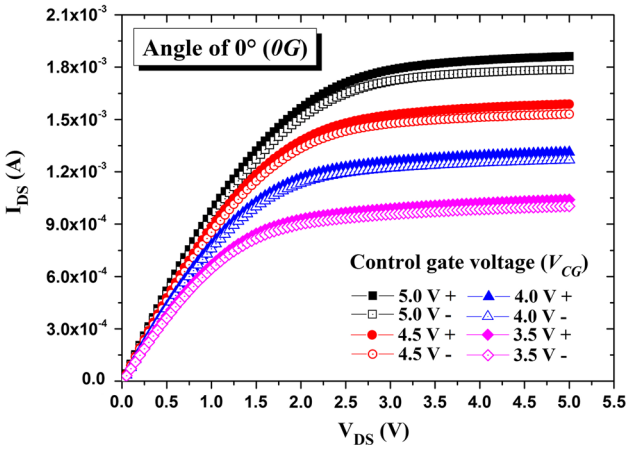

Fig. 15 FGMOS output curves, horizontal position (0°, 0G), where V_{CG} is the control gate voltage

Fig. 17), in order to apply an inertial force due to the gravity acceleration (G) and verify tilt sensing.

Corresponding output curves were obtained using a Keithley 4200A SCS parameter analyzer equipped with I–V Source Measure Units model 4210-SMU. The packaged chip was mounted on a tilt testing apparatus built in-house. Measurements were made extracting data from both transistors shown in Fig. 8. Measurements were made sweeping V_{DS} from 0 to 5 V and varying the control gate voltage V_{CG} from 3.5 to 5 V in 0.5 V steps, first with the chip resting in horizontal position (0°), since it is intended to test the device as a tilt sensor.

From Fig. 15 different observations can be obtained. A misalignment of the structure, probably due to the micromachining process, is observed, inferred from the output curves. When in horizontal position (0G), the drain current

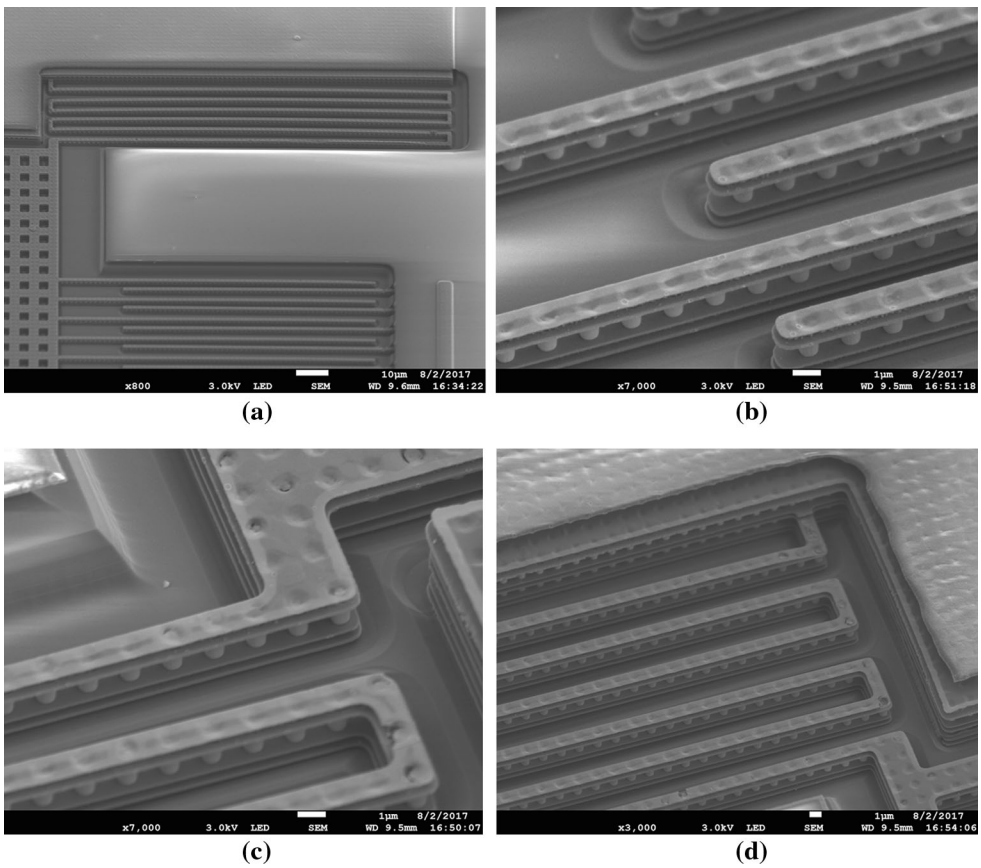

Fig. 14 SEM photographs of surface micromachining results; **a** capacitive structure and spring; **b** detail of the micromachined fingers; **c** detail of metal 1-metal 2 stack after etching; **d** detail of the link of the springs with the proof mass and comb fingers array released after etching

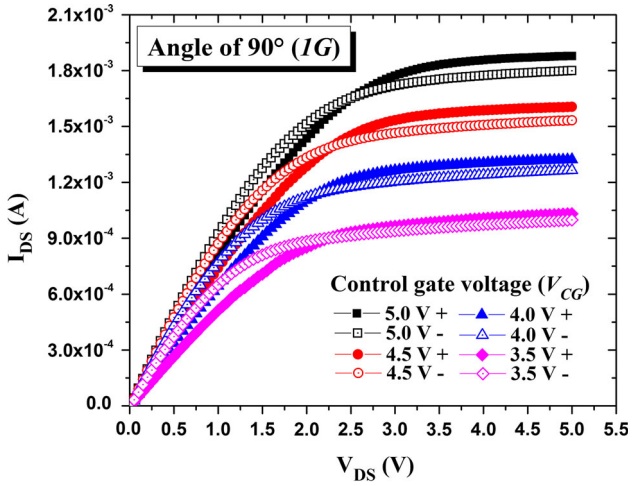

Fig. 16 FGMOS output curves, 90° tilt (1G), where V_{CG} is the control gate voltage

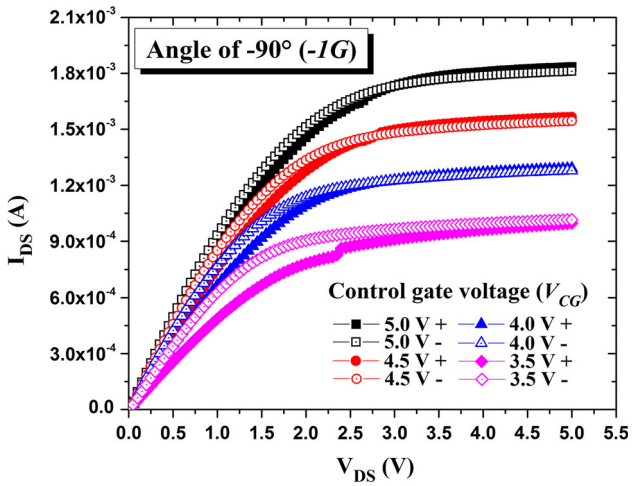

Fig. 17 FGMOS output curves, − 90° tilt, where V_{CG} is the control gate voltage

from both FGMOS transducers should be equal. It is also observed that the lower the drain voltage, the less noticeable the effect of misalignment is. The filled symbol corresponds to the transistor used to sense positive acceleration and the outline symbols corresponds to the transistor used to sense negative direction.

Next, Fig. 16 shows that the level of drain current flowing through the FGMOS transistor to sense positive acceleration (+) is higher compared to the drain current of the opposite transistor dedicated for sensing negative acceleration (−) when the device is tilted 90° subjected to 1G acceleration, as was expected.

Finally, Fig. 17 shows that current levels are reversed compared with Fig. 15, corresponding to the new position, as expected. It should be noted that since the current begins in a lower level for the transistor made to measure positive displacement (270°, − 1G), compared with its opposite transistor, the current difference is less, however a current change is still present. This is caused by the asymmetry included in the design, to differentiate the direction of the displacement.

These results show that a mechanically variable coupling coefficient can be configured into an FGMOS, delivering different current magnitudes with a fixed operating point established. Also, although a variable capacitance is used too in commercial accelerometers, a direct correlation from capacitance variation into current can be obtained in a simpler way. This was achieved using a standard CMOS technology, completed with a very simple surface micromachining procedure to release the proof mass.

As this work was intended for an initial evaluation of the possibility to have a variable coupling coefficient related to FGMOS transistors, complementary work is still ahead to include characterization to obtain common parameters usually shown by commercial accelerometers like sensibility, G range, dynamical sensing response, frequency operating range, sensor resonant frequency and operating voltage range, among others. Also, this complementary work should include a structure design optimization for more reliable outputs, or even using the polysilicon layers as the structural layer of the inertial sensor.

7 Discussion

These experimental results can give indication that it is possible to use a capacitive structure based on comb fingers to configure a variable capacitor that can be embedded within a FGMOS transistor. Conventional inertial sensors based in a comb finger capacitive array make use of lateral area of the structural layer, which is completely solid and depends on the thickness dictated by the dedicated MEMS technology (PolyMUMPS, for instance).

On the other side, CMOS technology offers thinner metal layers that can only be stacked through vias, so lateral capacitor plate's area is not solid, as is shown in Fig. 13. This can be the reason why there is a rather small current difference in different static sensing positions.

However, it is a fact that an FGMOS with a variable coupling coefficient can operate as an inertial sensor, as these results show. Work should still be done to optimize the mechanical sensing structure and the optimum operating point for the FGMOS, as well. Although this work demonstrates a variable coupling coefficient principle in a very basic way, this can be used to develop structures that may correlate movement with an output electrical signal in a simpler way than that used conventionally.

8 Conclusion

A FGMOS transistor can be used as a transducer device in order to correlate inertial force and electric current. This gives to the FGMOS a different application, apart from those usually used as a digital memory or variable resistance device in artificial neural networks, for instance. An electromechanical inertial sensing structure was designed and fabricated, including a surface micromachining post-process to obtain a CMOS-MEMS inertial sensor. It was demonstrated that a FGMOS with a variable coupling coefficient can be achieved by mechanical means. Hence, it was shown that despite the characteristics of the structural layer used in this accelerometer, displacement can also be sensed, based on a standard CMOS technology. Testing was carried out in different positions and operating conditions, showing that the conversion from displacement to current using an FGMOS transducer is possible. The operating voltages for which the device is sensitive to changes in position are compatible with those commercially available. Moreover, the test demonstrates the feasibility of dynamically change the coupling coefficient in an FGMOS to alter its current behavior in real time, by embedding this device in an electromechanical structure.

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