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Methodology for Design, Measurements and Characterization of Optical Devices on Integrated Circuits

G. Castillo-Cabrera[1,3], J. García-Lamont[2] and M. A. Reyes-Barranca[3]
[1]Superior School of Computing (ESCOM), National Polytechnic Institute (IPN),
[2]Institute of Basic Science and Engineering, CITIS, Hidalgo State University,
[3]Electrical Engineering Department, SEES, CINVESTAV-IPN,
Mexico

1. Introduction

The main application of optical devices is image processing which is a research field still in study for a wide variety of applications, such as video digital cameras for entertainment use, pattern recognition based in artificial neural networks, real time object tracking, clinical uses for repair by stimulation parts of visual system and artificial vision for application in silicon retinas, among others. So, it is important to evaluate the performance of available integrated photo-sensor devices used in these applications, considering issues as noise, resolution, processing time, colour, etc. Actually, there are several technologies available for integration of photo devices, commonly CCD, BiCMOS and GaAs. Although all of them are usually applied in image acquisition systems, there are still some performance aspects that should be optimised, as voltage levels, leakage currents, high fabrication costs, etc., so research is still being done to overcome these limitations. Standard CMOS integrated circuit technology is also an attractive alternative, since devices like phototransistors and photodiodes can be implemented as well. The foremost advantage of CMOS devices is its availability in standard technology. It should be mentioned that this technology has also some limitations but since fabrication of CMOS integrated circuits has low costs, exploration of the potential of new technologies for image processing is still an interesting field. Besides, algorithms can be implemented along for tasks such as border detection (space vision), movement detection (space-time vision), image enhancement (image processing vision) and pattern classification or recognition (neuro-fuzzy vision).

Considering the state of the art (Aw & Wooley 1996; Storm & Henderson, 2006; Theuwissen, 2008), as well as clinic approaches (Zaghloul, & Boahen, 2004), in this work, a chip was designed and fabricated, with two possible photo-sensor structures: *p+/N-well/p-substrate*, for phototransistors and *N-well/p-substrate*, for photodiodes, through the standard 1.5μm AMI's- , *N-Well* technology. In the future, it is the intention to design a second chip that must include electronics for image processing with pulse frequency modulation (PFM), once the characterization gives enough information about the performance of the stages studied. A complete description is given.

2. Devices Involved, type of structures

After the CCDs, the new generations of optical devices are based in standard CMOS technology. Experimental study based is here presented, about two typical structures in the field of art, namely, phototransistor and photodiodes which were designed and fabricated through the standard 1.5µm AMI's- technology. Technically those are known as "structures P+/N-Well/P-substrate" and "structures N-Well/P-substrate" respectively, which are presented by Fig. 1.
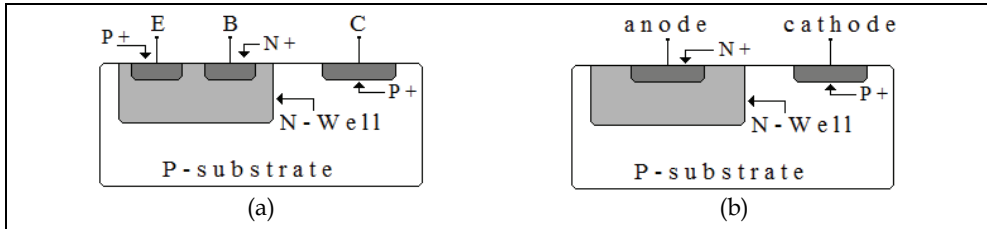

Fig. 1. Optical devices, (a): P+/N-Well/P-substrate, (b): N-Well/P-substrate

In the former, Fig. 1(a), P+/N-Well/P-substrate, the P+/N-Well is being an active junction as well as N-Well/P-substrate junction. An active junction is one in which two semiconductors with different conductivity, "p" and "n" type, are joined and electrically interacting. N-Well is a diffused region n-type on substrate. P+ on N-Well is an implanted material and also serves as low resistive ohmic contact. N+ on N-Well is an n-type implanted region and solely is used as low resistive ohmic contact. P+ on P-substrate is an implanted p+-type material and is used as low resistive ohmic contact. Terminals E, B and C are Emitter, Base and collector respectively in the phototransistor.

In the last one, Fig. 1(b), N-Well/P-substrate, there is only one active junction. N+ and P+ are implanted regions which does low resistive ohmic contact with N-Well and P-substrate respectively.

Both, structures P+/N-Well/P-substrate and N-Well/P-substrate, symbols are presented by the Fig. 2.
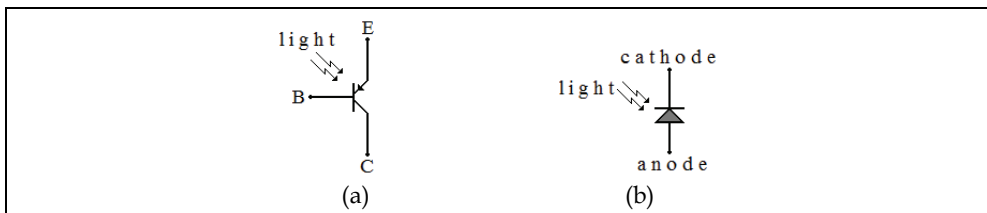

Fig. 2. Symbols for optical structures (a): P+/N-Well/P-substrate, (b): N-Well/P-substrate

3. Circuital architecture of pixel for characterization

3.1 Components of architecture

Fig. 3 presents the pixel architecture which has resulted efficient for optical devices characterization. It consists in optical device, four transistors, a source of current and buffer

for readout. The common source amplifier consists, in M1 transistor and current source Isc, and it is used to handle the photocurrent. M2 is row select transistor and is not part of amplifier strictly speaking, however its position play an important role on this architecture, as will be shown in section 4. Photocurrent, from optical device, is integrated at the parasitic capacitance of the p-channel transistor M1, between node 2 and substrate, which is tied to ground. Assuming that photocurrent is constant, the relation of integrated voltage can be obtained by using the relation $q = C \cdot V$ in the parasitic capacitance.

$$V_{int} = \tfrac{1}{C} \int_0^{\Delta t} i \, dt \qquad (1)$$

where

$$i = \tfrac{dq}{dt} \qquad (2)$$

MSHUT along with signal VSHU controls the exposition time Δt. MREST along with signal VRES have as function to reset the nodes 1 and 2 at level Vreset. Optical devices can be P+/N-Well/P-substrate or N-Well/P-substrate structures. BUFFER OUTPUT provides power to avoid disturbance during readout.
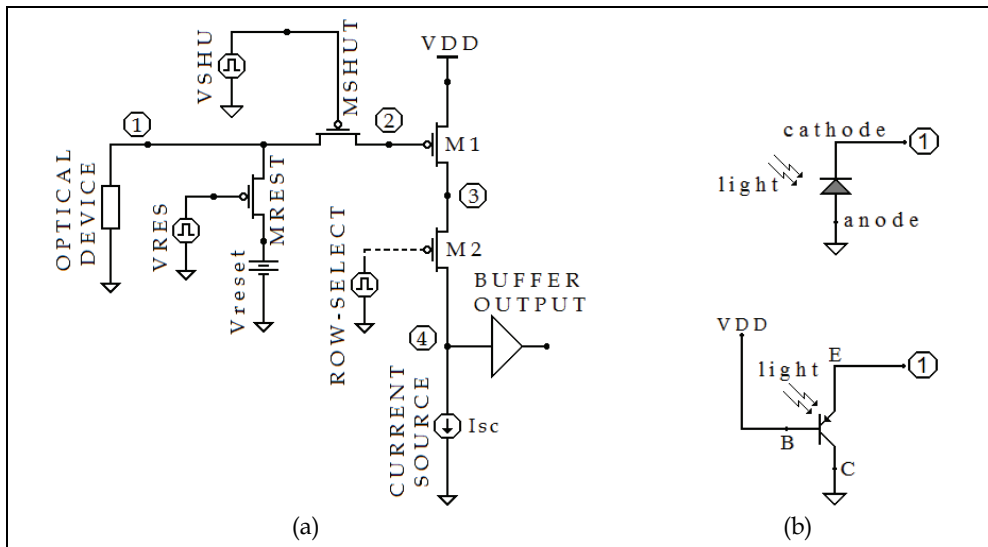

Fig. 3. (a) Architecture of pixel, (b) Optical device

Transistors MSHUT and MREST operate as switches in order to integrate the photocurrent generated in the photo-sensor at a given time and operation frequency. Fig. 4 shows the waveforms of their respective gate voltages. Integration time Δt, takes place while MSHU is on and MRES is off. During this time, the photocurrent is converted to voltage at the gate of transistor M1 (node-2 in Fig. 1). The relation between the integrated voltage and photocurrent is expressed in Eq. (1), assuming that the photocurrent is uniform in time. The DC voltage source, Vreset, is the reference voltage from which integration of the photocurrent is carried out.
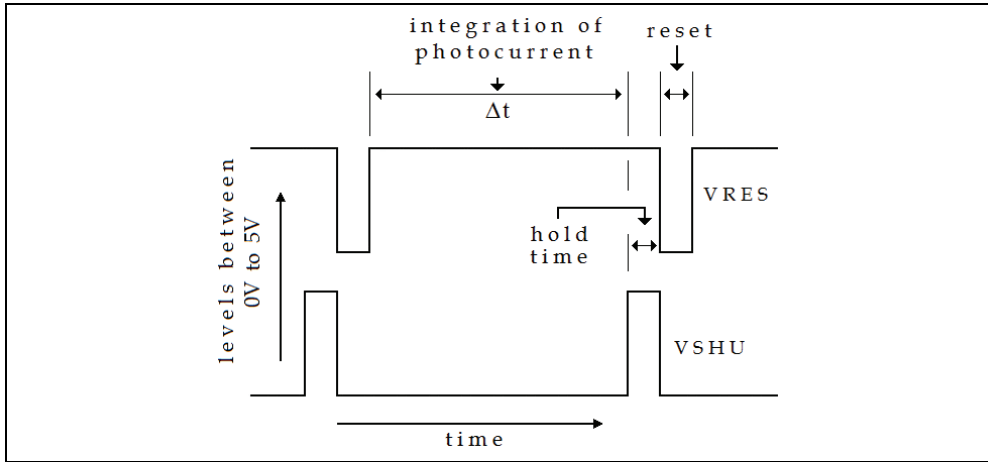
3.2 Signals of control

Fig. 4. Waveform of signals shutter and reset

$$I_{ph} = C_T \left(\Delta V_{\text{int}} / \Delta T \right) \tag{3}$$

where:

I_{ph} :   photocurrent from the photo-device.

C_T :   capacitance at node-2

ΔV_{int} :   integrated voltage in C_T ($\Delta V_{\text{int}} = \Delta V_{measured} / Av$)

ΔT :   integration time

Av :   amplifier's gain

In addition, Vreset sets the quiescent point of the amplifier. Fig. 4 shows the input voltage pulses applied to the gate of MRES and MSHUT, respectively.

Since the objective of this work is to propose a methodology for the characterization of photo-devices and pixel architectures, the design was made considering those parameters affecting the performance of pixels and the way they will be measured. The design was carried out with the more simple architecture. Unlike what was reported with current amplifiers in the current-mode readout configuration (Philipp et al 2007), the amplifier is configured for voltage-mode operation in this work. From results obtained with this design, useful information can be processed and analysed considering a specific application, regarding factors such as the spectral response and silicon integration area of *p+/N-well/p-substrate* phototransistors and *N-well/p-substrate* photodiodes, as well as integration time, integrated voltage, transistors' aspect ratio and reference voltage used, for instance. Considerations about technology parameters, is important also in the definition of the dependence of the response and the architecture operation upon the photo-device structure.

Here, we present the electronic design, layout, simulations and some measurements on the fabricated chip. This prototype was made using the 1.5μm AMI's technology. The chip contains five pairs of phototransistors and five pairs of photodiodes, with one instance of each pair covered with metal for dark current characterization purposes. Results reported

here are only from those devices having an area of (9μm)x(9μm). Bigger photo-devices were also measured, but as they saturated the amplifier, no useful results were obtained. A drawing is given in the Fig. 5 which is showing the fabricated array.
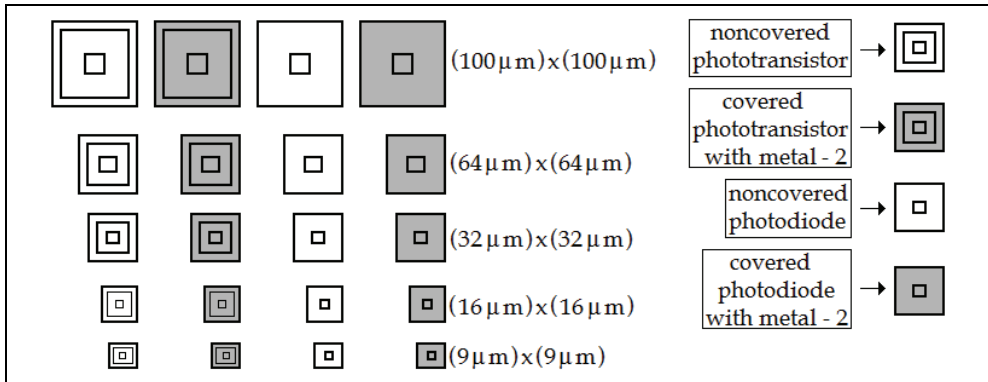

Fig. 5. Drawing for the array of optical devices

4. Circuit analysis

Now, doing reference to the Fig. 3, some design criteria for the circuit are defined. (1) Transistors MREST and MSHUT are used as switches, so their sizes can be drawn with minimum dimension features allowed by the technology. (2) Channel modulation effects must be avoided with M1, therefore its channel length should be at least five times the minimum dimension allowed. (3) For proper operation of the amplifier, it is recommended to choose a stable current source for biasing, thus, a cascode configuration was selected and designed for sourcing 20μA. (4) By adjusting the current source and Vreset the voltage gain of the amplifier it is varied, giving a useful degree of freedom for the characterization of the architecture and different devices, including the possibility another kind of not optical integrated sensors. (5) Transistor M2 it is inserted into the amplifier since it is a standard way for selecting row within an array. However, the role of M2 on the amplifier here proposed must be analyzed. (6) Finally, a standard buffer circuit is used for provide of power to the output.

Fig. 6 (a) shows the schematic of the cascode current source used for biasing the amplifier. Transistors involved in the amplifier are M1, M2, M4 and M6. Fig. 6 (b) shows the equivalent circuit for the amplifier and the cascode current source, used to find a mathematical relationship between the voltage gain and the size of M2.

From Figure 4(b), r_s is the channel resistance of M2; here, subscripts 01, 04 and 06 are identifiers for transistors M1, M4 and M6, respectively. A circuit analysis gives the following expression for the output voltage, V_{out} :

$$r_{01}i_1 + r_s i_2 + r_{04}i_3 + r_{06}i_2 = 0 \qquad (4)$$
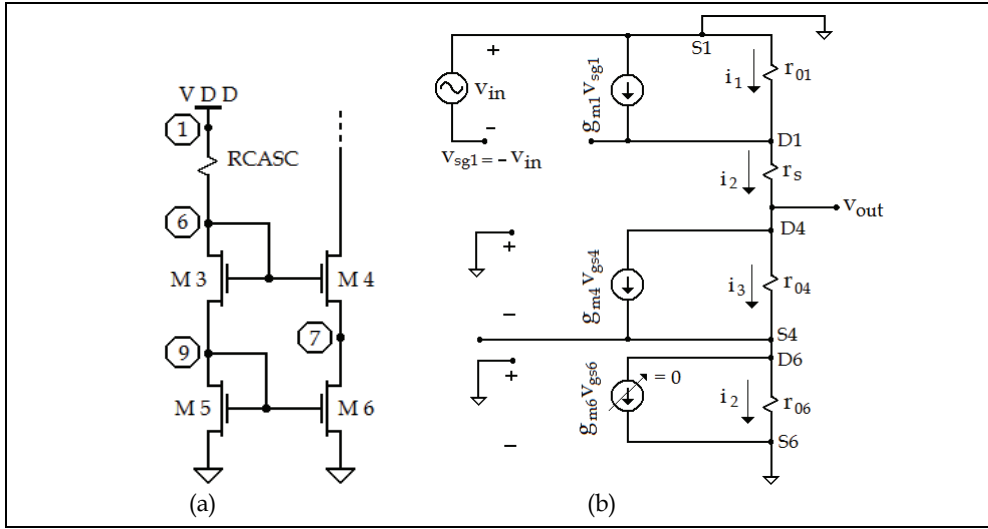
$$i_2 - i_1 = g_{m1}v_{sg1} \qquad (5)$$

Fig. 6. Cascode source current (a) schematic, (b) equivalent circuit

$$i_2 - i_3 = g_{m4}v_{gs4} \tag{6}$$

$$-v_{out} = r_{01}i_1 + r_s i_2 \tag{7}$$

$$v_{out} = r_{04}i_3 + r_{06}i_2 \tag{8}$$

Equations from (4) up to (8) are mesh equations from which the next expression is obtained:

$$R_0 i_2 = v_{out} \tag{9}$$

Where

$$R_0 = r_{04} + g_{m4}r_{06}r_{04} + r_{06} \tag{10}$$

$$-i_1 + i_2 = g_{m1}v_{sg1} \tag{11}$$

$$r_{01}i_1 + r_s i_2 = -v_{out} \tag{12}$$

And by using (11) and (12), i_2 can be obtained:

$$i_2 = \frac{r_{01}g_{m1}v_{sg1} - v_{out}}{r_s + r_{01}} \tag{13}$$

From (9) and (10), the voltage gain of the amplifier is deduced:

$$R_0 \left(\frac{r_{01}g_{m1}v_{sg1} - v_{out}}{r_s + r_{01}} \right) = v_{out} \tag{14}$$

Defining the next ratio:

$$K = \frac{R_0}{r_s + r_{01}} \tag{15}$$

$$r_{01} g_{m1} v_{sg1} K - v_{out} K = v_{out} \tag{16}$$

And since

$$v_{sg1} = -v_{in}$$

$$Av = \frac{v_{out}}{v_{in}} \tag{17}$$

Finally the voltage gain is obtained:

$$Av = -\frac{K}{K+1} r_{01} g_{m1} \tag{18}$$

When $K \gg 1$, the gain can be approximated to:

$$Av \cong -r_{01} g_{m1} \tag{19}$$

This is only possible if r_s is sufficiently small, from (15). So, assuming that $r_{01} = r_{04} = r_{06}$ from (10) and (11), the size of M2 must be such that r_s will result very small, compared with r_{01}, r_{04} and r_{06}. With an iterative procedure, the aspect ratio W/L of M2 was made large enough such that r_s does not have a strong influence over the amplifier's operation (Baker *et al* 2005). So, for the technology used the calculated aspect ratio for M2 was, $W = 64.8 \mu m$ and $L = 2.4 \mu m$. Then, considering these design outlines, the operation of the circuit based on M2 can be traduced in a convenient performance evaluation. As a result of the above design considerations, this basic analysis of the equivalent circuit reveals that the role of the row-select transistor is important for the proper operation of the amplifier. The voltage gain in (19) can be estimated using the following expressions (Baker *et al* 2005):

$$r_{01} = \frac{1}{\lambda \cdot I_D} \tag{20}$$

$$g_{m1} = \sqrt{2(KP)\frac{W}{L} I_D} \tag{21}$$

Using values of KP and λ, from the 1.5μm AMI technology, the maximum voltage gain was estimated as: $Av = 35 dB$.

4.1 Simulation
Once the sizes of transistors used in the pixel were calculated, simulations with PSPICE were made to confirm the behavior of the circuit. Fig. 7 shows the gain range that can be achieved with the amplifier, going from 10dB to 32dB. Beside this, Input voltage, which is provided with Vreset, goes from 2.2V up to 3.5V, taken as parameter RCASC in the source current, Fig. 6(a).
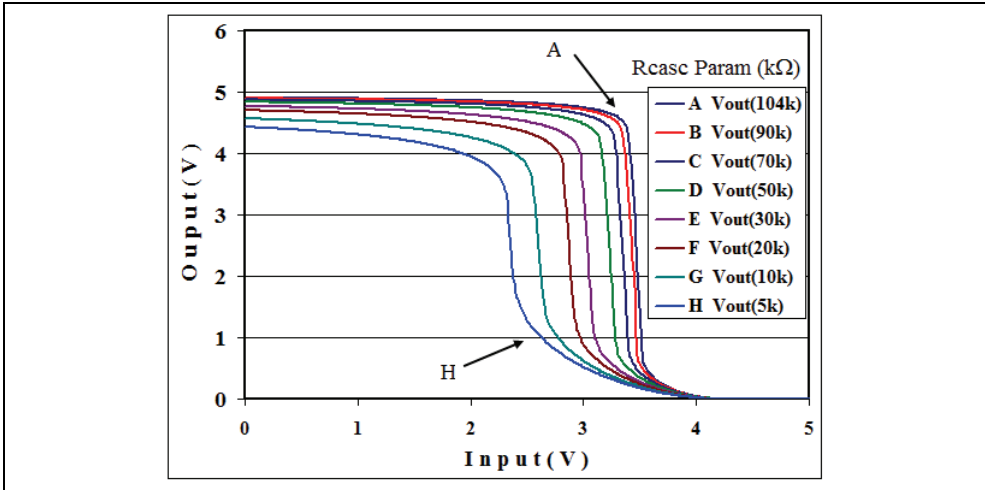
Fig. 7. Transfer function simulated

In order to evaluate temporal response, input voltage was adjusted to 3.5V, which belong to the gain of 32dB. Fig. 8 shows a simulated temporal response. Time of integration is of 0.9ms and time of reset is 0.1ms, according with the waveforms of VSHU and VRES seen in the Fig. 4. Level of photocurrent for simulation was taken of 10pA, from Reginald-Krishna's model (Perry 1996).
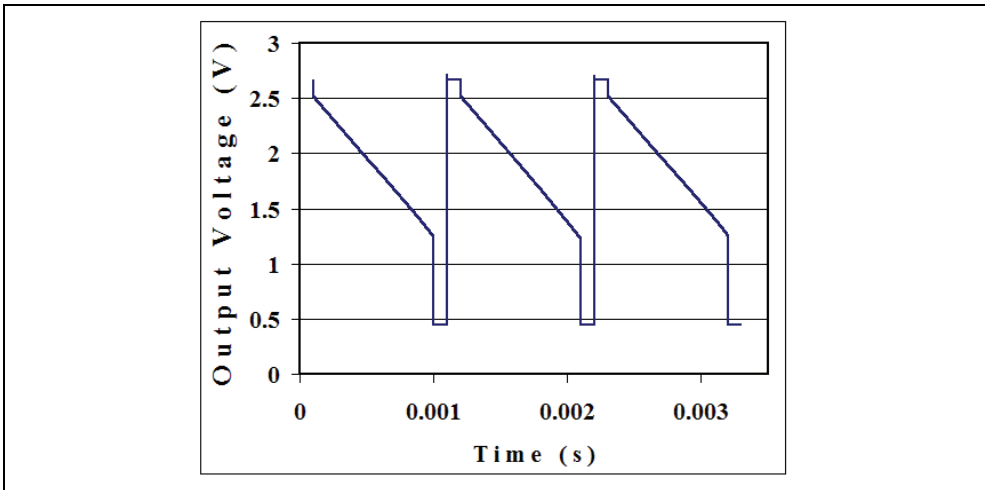

Fig. 8. Temporal response structure P+/N-Well/P-substrate

4.2 Layout

Cross section and layout are given in Fig. 9 and 10, for P+/N-Well/P-substrate and N-Well/P-substrate structures, respectively.
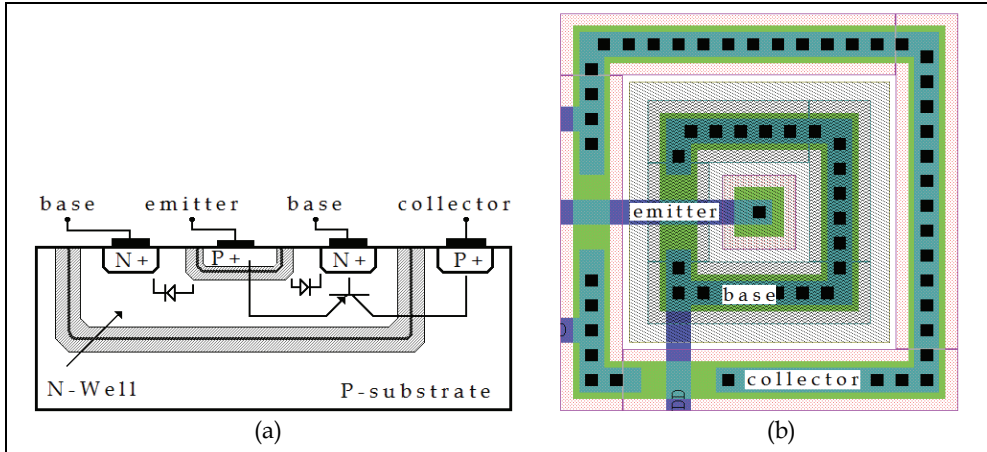
Fig. 9. P+/N-Well/P-substrate structure (a) Cross section (b) Layout

We can see two junctions in the Fig. 9. As it was been established in the Fig. 3, terminal of "emitter" is periodically reset at CD level of Vreset, which is also the amplifier´s point of operation. Terminal of "base" is tied to VDD which is power supply. "Collector" is tied to ground. Both junctions are biased in reverse way. Base-emitter junction is to (5V-Vreset) and base-collector junction to (5V-0V).
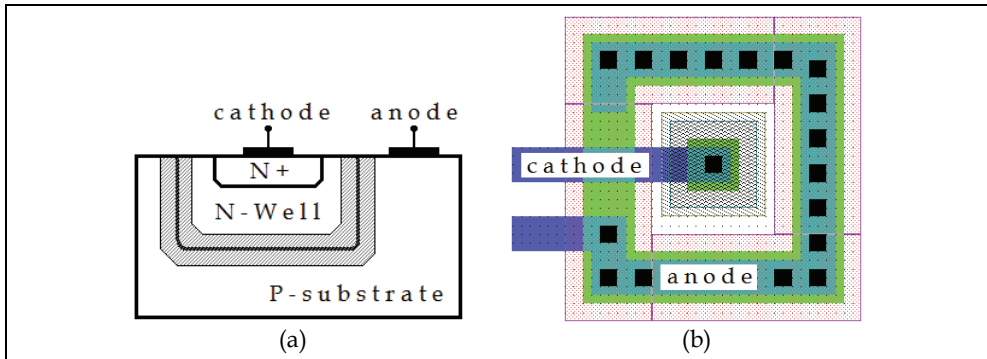

Fig. 10. N-Well/P-substrate structure (a) Cross section (b) Layout

Photodiode, structure N-Well/P-substrate given in Fig. 10, only has two terminals. Terminal of cathode is reset to Vreset periodically and anode is tied to ground. So, it is biased in reverse way.

The phototransistor's "base" has the same dimensions of the photodiode's anode ring, (9µm)x(9µm). So, both has the same active surface. The photocurrent generated is collected by the phototransistor's emitter and the same happens with the cathode of the photodiode.

5. Results

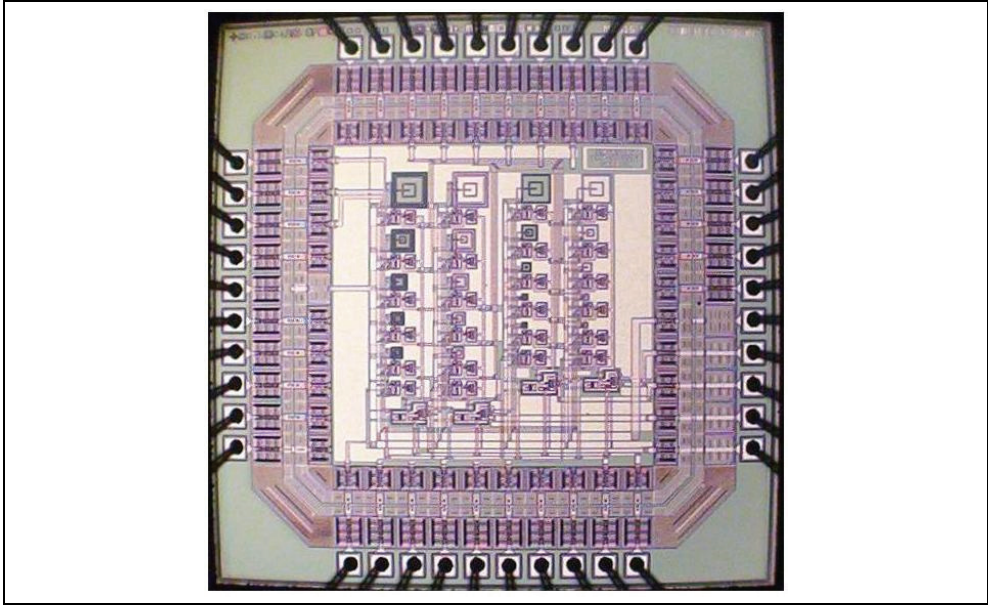An array, which has been drawn in the Fig. 5, was fabricated and it is shown in the Fig. 11.

Fig. 11. Fabricated array of devices, microphotography

At the bottom of each column we can see a block, which comprise both, cascode source current Isc and BUFFER OUTPUT. First left column has different size of not covered phototransistors, P+/N-Well/P-substrate structures. Second column of left to right consists of P+/N-Well/P-substrate structures, similar sizes that first left column but covered with metal 2 (process AMI of 1.5µm). Third and fourth columns of left to right are not covered and covered N-Well/P-substrate structures respectively, photodiodes. Transfer function measured, of amplifier is given in the Fig. 12.
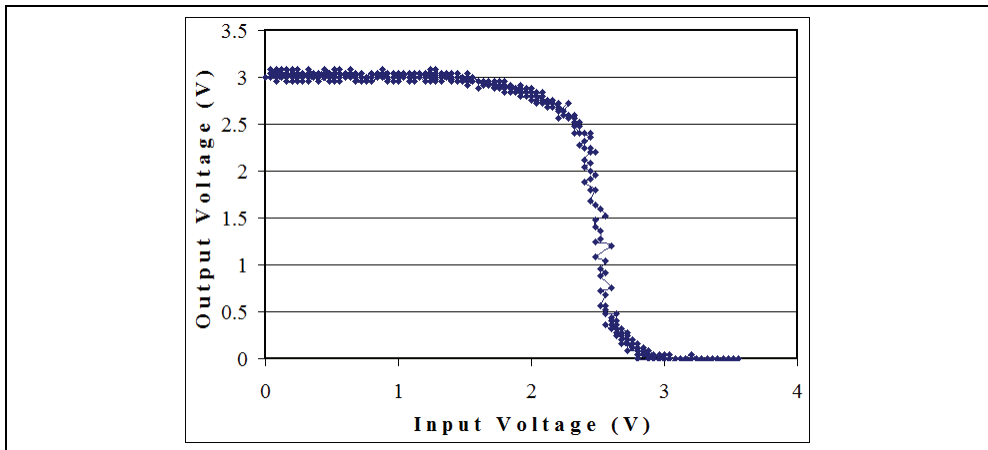

Fig. 12. Experimental transfer function of amplifier

Experimental transfer function of amplifier is quite fitted to the criteria design. Fig. 12 shows one of these functions. During the procedure of calibration, in a first set of measurements it was saw a strong response in the case photodiodes. So, in order to carry out measurements, the amplifier gain was set at 10dB in case of photodiodes measurements, while phototransistors at 32dB, in order to have a good reading without saturated response. It is clear that response of the photodiode, shown in Fig. 13 tend to be much larger than phototransistors, Fig. 14. This is an indication that the integrated current within the photodiode is higher compared to that of the phototransistor, even with the same incident illumination power.
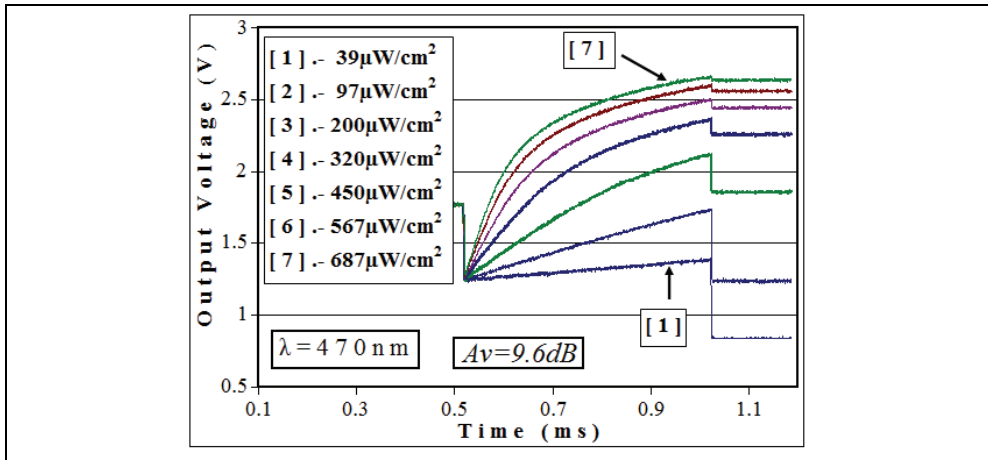
Fig. 13. Measurements of the temporal response in the N-Well/P-substrate structures (photodiodes)
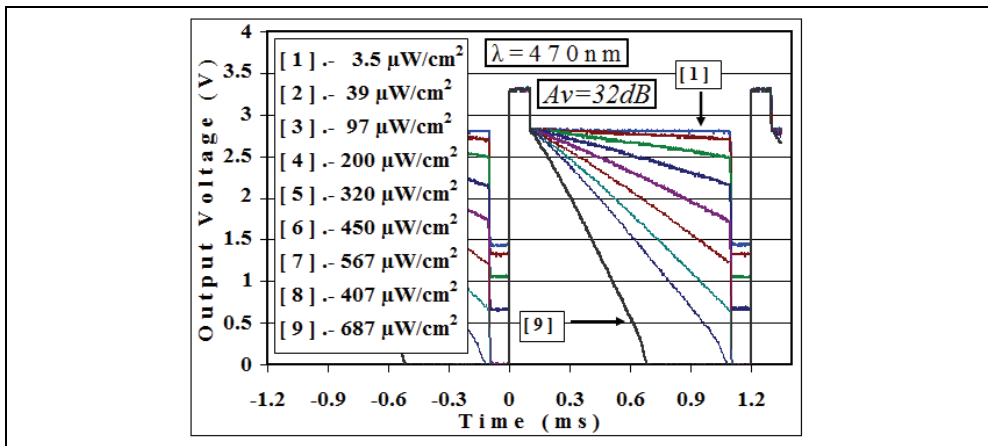
Fig. 14. Measurements of the temporal response in the P+/N-Well/P-substrate structures (phototransistors)

This is confirmed with the plots shown in Fig. 15 and 16, where the photocurrent was estimated as a function of wavelength. The difference between each other is about one order of magnitude. These responses were carefully obtained adjusting the gain of the amplifier and with experimental data of sensitive surface, capacitance in the node 2 and integration time. The photocurrent was estimated using equation (3) and similar data from Figure 13 and 14. Here, the technology spread can be seen also as five chips were measured giving some dispersion from each photo-device measured. As result, a display logarithmic is shown in Fig. 17. A monochromator HILGER & WATTS and an ISA lamp were used. Characteristic spectral for that lamp, used in this work, is shown in the Fig. 18.
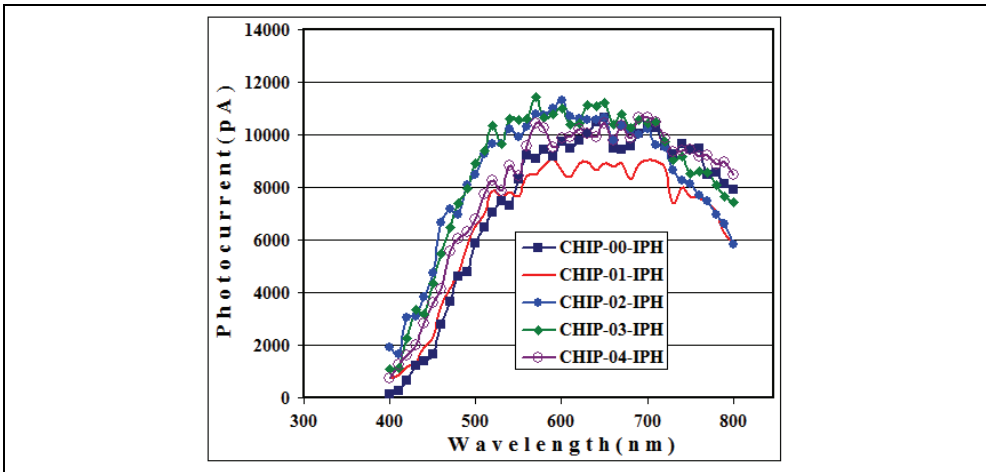

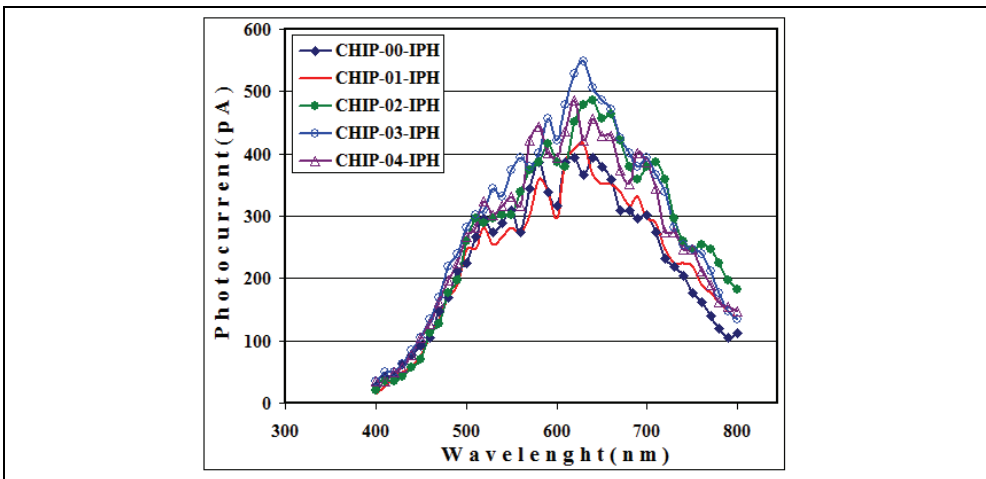Fig. 15. Spectral response of N-Well/P-substrate structures (photodiodes)

Fig. 16. Spectral response of P+/N-Well/P-substrate structures (phototransistors)
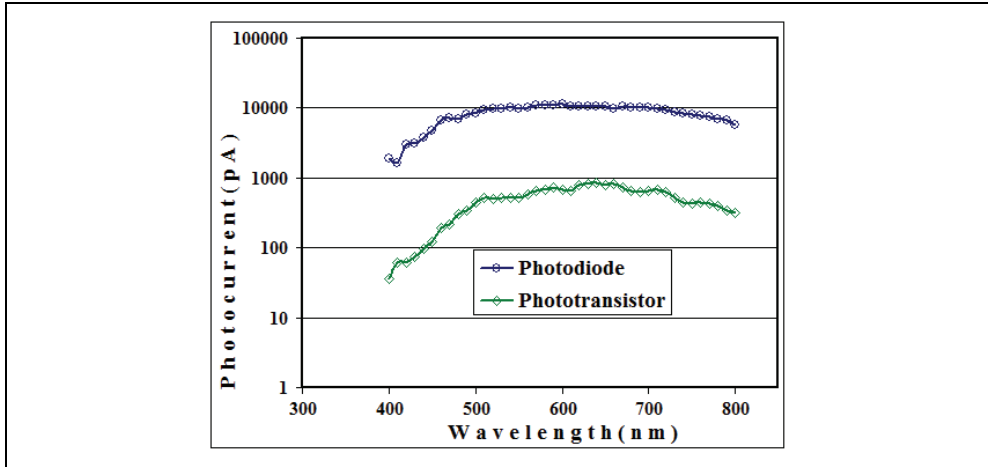
Fig. 17. Spectral response in logarithmic scale of P+/N-well/P-substrate (phototransistors) and N-Well/P-substrate (photodiodes), structures.
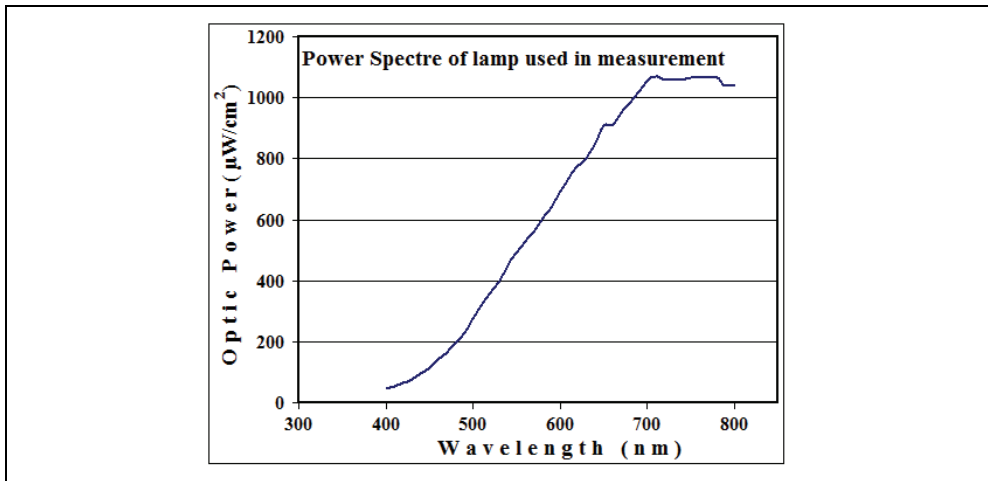

Fig. 18. Power spectre of lamp ISA used for measurements

A kind of small oscillations can be observed from Fig. 15 and 16. It has been suggested these oscillations are due to the Fabry-Perot interference (Lee *et al* 2007, Liang *et al* 2001). For both (9µm)x(9µm) phototransistors and photodiodes, the spectral response was measured. Fig. 17 presents a comparison in magnitude between the spectral responses of phototransistors and photodiodes. Again, it can be seen that the photocurrent from the photodiode is higher than the photocurrent from the phototransistor. Fig. 19 shows a comparison among the spectral response of the phototransistor used in this work (with 500 µW/cm² optical power) and the reported Reginald-Krishna's model (Perry 1996) using two other alike photodiode structures.
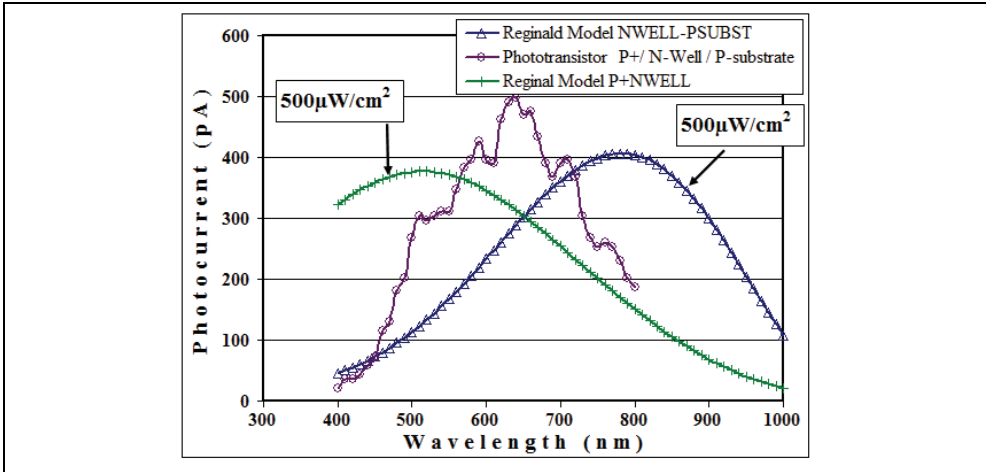
Fig. 19. Spectral response P+/N-Well/P-substrate vs. Reginald-Krishna's model of P+NELL and NWELL-PSUBST (Perry 1996).

It should be noted that the experimental photo-response of the P+/N-Well /P-substrate structure (phototransistor) has its maximum just where the junctions NWELL-PSUBST and P+NWELL models overlap. The model's plots are ideal optical response of the indicated junctions, so they do not include parasitic currents generated by additional events as crosstalk, for instance.

Crosstalk is a problem that can be present with neighbouring illuminated pixels that collect reflected or refracted light through lateral paths. Ideally, this should be avoided to minimize the degradation of pixels. Crosstalk can increase if integration density of pixel arrays is increased as technology shrinkage the size of devices. Then, the experimental curve is shifted toward the right from the ideal P+NWELL curve. It should be remembered that the emitter-base junction is the active one in the phototransistor. Fig. 13 (a) and (b) show photosensitivity and quantum efficiency respectively, for the measured phototransistors. The experimental photocurrent density was evaluated with Eq. (22).

$$J_{ph} = \frac{C_T \cdot \Delta V_{in}}{A_{ph} \cdot \Delta T} \qquad (22)$$

Where:

J_{ph} :   photo-sensor current density.

C_T :   capacitance at node-2.

ΔV_{in} :   integrated voltage at node-2.

A_{ph} :   sensitive area of the phototransistor.

ΔT :   integration time according to Figure 2.

The photosensitivity was evaluated using the following expression:

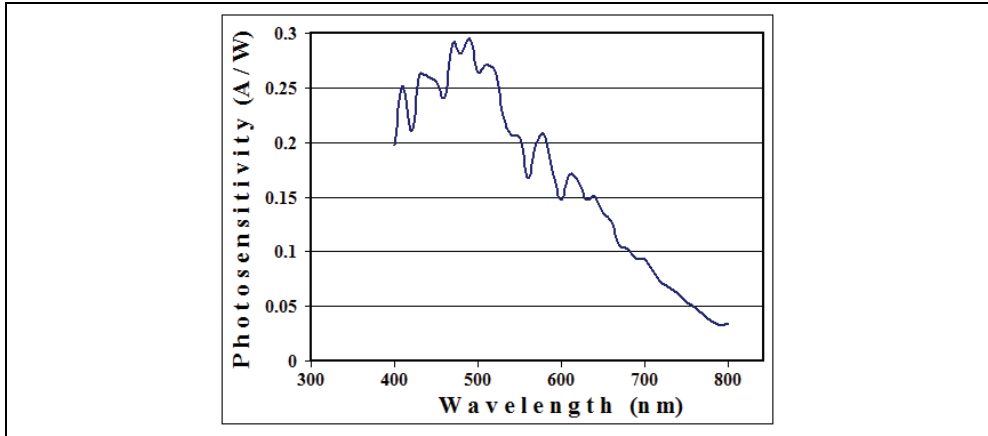$$S_\lambda = \frac{J_{ph}}{P_{opt}} \qquad (23)$$

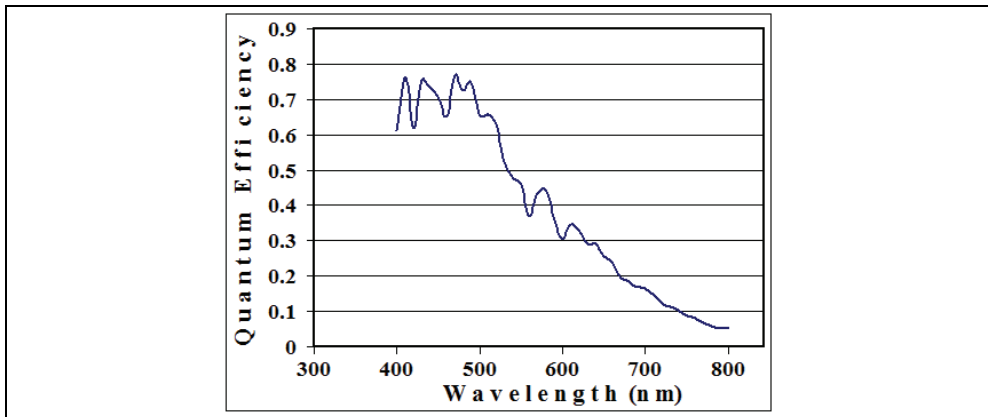Fig. 20. Photosensitivity of P+/N-Well/P-substrate structure

Fig. 21. Quantum efficiency of P+/N-Well/P-substrate

Where

P_{opt} :   optical power density from Figure 11(b).
The quantum efficiency QE was evaluated with:

$$QE = S_\lambda \frac{h \cdot c}{\lambda \cdot q} = 1240 \frac{S_\lambda}{\lambda} \qquad (24)$$

and

$h \cdot c / \lambda$: energy of photons, with λ in μm.
q :   charge of electrons.

6. Discussion

Temporal response shown in Fig. 13 and 14 were made using a fixed wavelength with optical power as a parameter. After several test over the photo-devices, 470 nm was selected

for measurements since this wavelength gave the maximum sensitivity, as can be seen from Fig. 20. With the structures used as photo-devices, a strong difference of the spectral photo-response between phototransistors and photodiodes can be identified. It can be seen from Fig. 17 that for same illumination conditions, the response of photodiodes is higher than the response of phototransistors, by almost one order of magnitude. Moreover, measurements were made also over structures covered with a layer of metal, and the results are shown in Fig. 22, 23 and 24 for phototransistors and photodiodes, respectively. In the case of phototransistors, it is seen that the response of covered devices is almost 85% weaker than that of a not covered device.

In the case of photodiodes, this difference is lower about 30%, what is due to a big substrate leakage current by the properties of the N-well/p-subs structure, which may have other contributions adding to carriers directly generated by photons from inside of the photodiodes' area. However, all of the measured current is stimulated by photons as we can see from Fig. 24(b). Furthermore, it can be suggested that the N-well/p-subs structure used
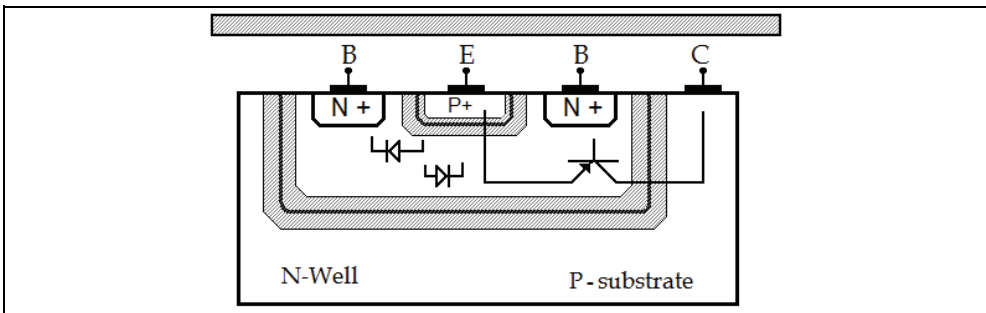

Fig. 22. Cross section of covered structure P+/N-Well/P-substrate structure, by metal 2 (phototransistor)
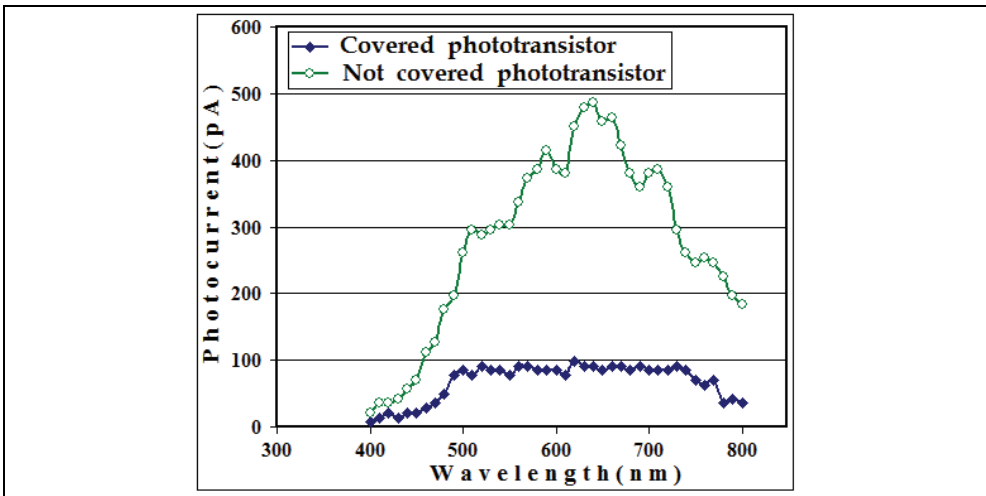

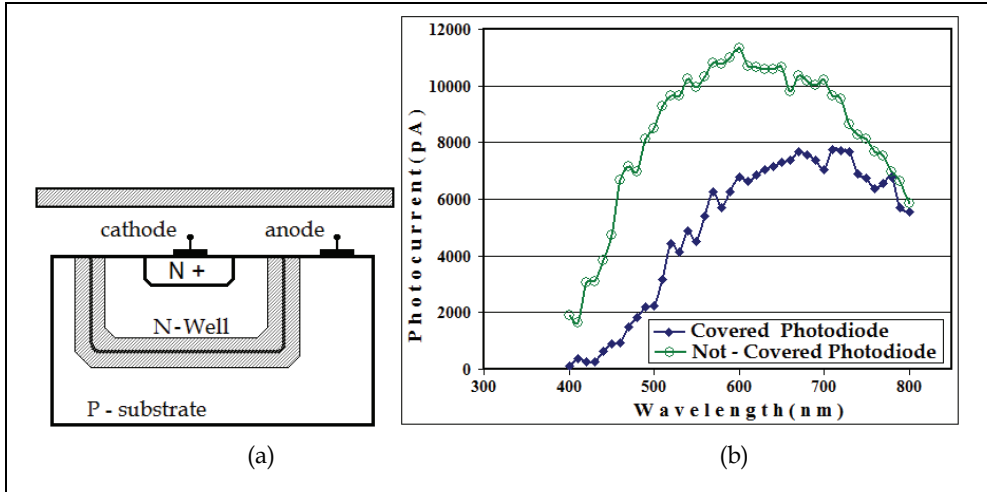Fig. 23. Response of covered and not covered phototransistors

Fig. 24. Photodiode, structure N-Well/P-substrate: (a) cross section, (b) response on covered and not covered device

as a photodiode is not too efficient due to crosstalk, degrading pixel's characteristics as the dynamic range and increasing the fixed pattern noise.

It is reported that crosstalk is a mechanism that is pronounced at longer wavelengths (Lee 2008) since light with these characteristics can go deep into silicon having a high probability to be reflected by the different layers present in the structure of the pixel. This can be confirmed with Fig. 24(b), where it is seen that the photocurrent of a covered photodiode increases as wavelength is increased. Furthermore, comparing Figs. 23 and 24(b), it can be concluded that the base-collector junction of the phototransistor operates as a barrier for carriers generated by light that penetrates beyond the surface region into the substrate. Since the photodiode has not this additional junction, it is collecting extra carriers, thus inconveniently reducing the difference between the response of covered and not covered devices. This should be considered also when designing pixel architectures, providing the pixel with surrounding materials with low dielectric constants and index of refraction, as long as the technology allows it. Otherwise, junction barriers as base-collector in phototransistors can play a similar role. Due to the importance of this mechanism over the performance of pixels, following an explanation is given regarding crosstalk.

6.1 Crosstalk mechanisms

We have focused in the characterization and analysis of likely mechanisms that could contributes to the crosstalk on structures "P+/N-Well/P-substrate" (phototransistors) and "N-Well/P-substrate" (photodiodes). On these kinds of photo-devices, crosstalk has been defined and classified in two main mechanisms: (a) optical crosstalk and (b) electrical crosstalk (Brouk 2002, Kang 2002, Tabet 2002). Here, we introduce an additional classification of crosstalk, as is shown in the Fig. 25 and 26. The first classification is the lateral crosstalk mechanism which includes lateral optical crosstalk, and lateral electrical crosstalk. The second one is the vertical crosstalk mechanisms.

Crosstalk mechanisms	
Lateral crosstalk mechanisms	Lateral optical crosstalk mechanisms
	Lateral electrical crosstalk mechanisms
Vertical crosstalk mechanisms	There aren't vertical optical crosstalk mechanisms
	Vertical electrical crosstalk mechanisms

Table 1. Crosstalk mechanisms classification

6.2 Lateral crosstalk mechanisms

Lateral optical crosstalk is due to light traveling laterally among the layers up to the junction (near the surface of the device) acting as a waveguide, as is shown in the Fig. 25. Lateral electrical crosstalk is the phenomenon whereby photons generate carriers in the "**near to the surface region**". That phenomenon has its origin in short wavelength light, mainly under of 650nm. Both, optical and lateral electric crosstalk, are present either in, phototransistors or photodiodes. However, in phototransistors this contribution is as a photocurrent collected by the base contact, which is tied to VDD, hence masking the effect. This is a first reason whereby the photo-current is larger in photodiodes than in phototransistors. Fig. 25(a) shows the way in which both, optical crosstalk and lateral electric crosstalk mechanisms, affect the response of phototransistors and Fig. 25(b) shows the corresponding for photodiodes. The effect is very strong since the current comes from all directions.
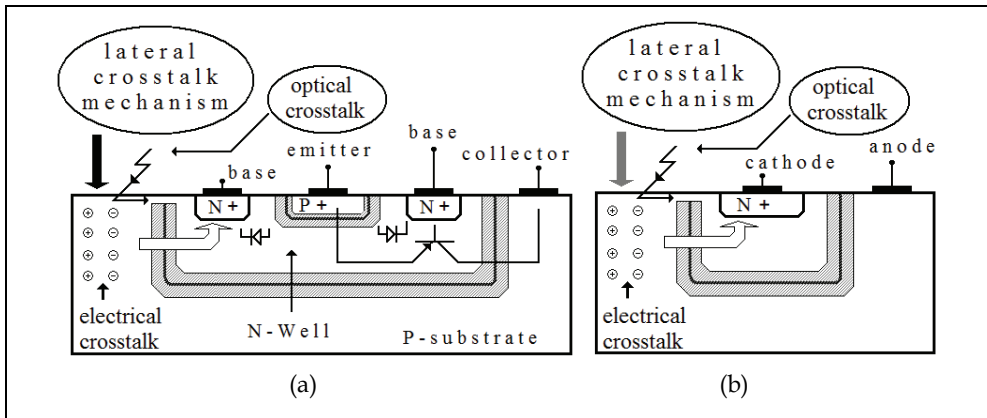

Fig. 25. Lateral crosstalk mechanisms in phototransistor

6.3 Vertical crosstalk mechanisms

Vertical crosstalk mechanism is shown in Fig. 17. It originates only due to electrical crosstalk, so it is called vertical electrical crosstalk. In the case of phototransistors, carriers generated along the substrate, as well as behind and outside the "N-Well", are collected by the base contact since it is connected to a higher voltage than the emitter (see Fig. 17(a)). So, only majority carriers are collected by the base.

In this case, diffusion of minority carriers is present as leakage current. Hence, little or no contribution to the spectral response of phototransistors is due to vertical electrical crosstalk.
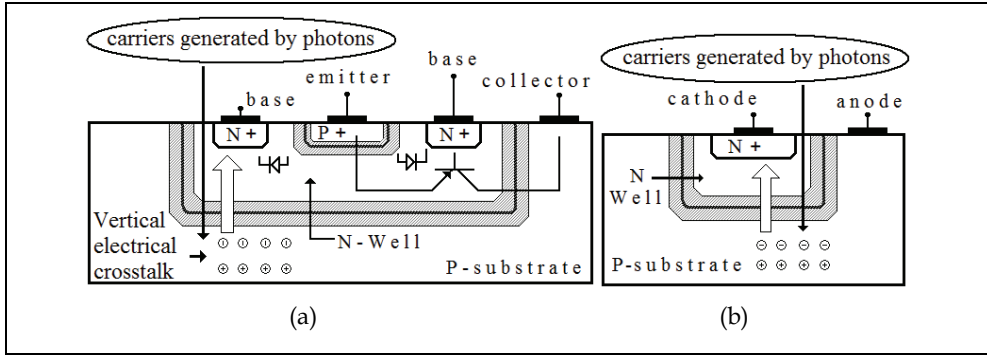
Fig. 26. Vertical crosstalk mechanisms in photodiode, (a) Phototransistors (b) photodiodes

Vertical electrical crosstalk effect in photodiodes is illustrated in Fig. 26(b). Carriers generated by photons behind and outside the N-Well contribute to the spectral response of the photodiode with the leakage current coming from the substrate. Carriers generated deep in the substrate are due to longer wavelengths. This component of leakage current has a very strong effect over photodiodes but this is not the case for phototransistors, so the difference appreciated in Fig. 17 can be attributed to this.

7. Conclusions

An architecture was proposed, from which characterization of photo-devices can be made, giving useful information for the performance evaluation of junction structures available in CMOS standard technologies. An adjustable gain amplifier, with a gain range of 10dB - 32dB, was configured allowing different biasing and operating points for photo-response measurement of different devices. Good agreement between simulated and experimental transfer function of the amplifier was obtained. The row-select transistor, M2, plays an important role in the operation of the amplifier. It was found that the aspect ratio of this transistor should be high in order to have a small channel resistance and to ensure an adjustable gain property to the amplifier. On the other hand, phototransistors (p+/N-well-/p-subs) and photodiodes (N-well/p-subs) were characterized for a 1.5µm technology, but the same methodology can be used with other silicon foundries. Structures have a maximum quantum efficiency of about 0.7 and a maximum sensitivity of almost 0.3A/W. Besides, photodiodes made with an N-well/P-subs junction, have shown a strong substrate leakage current contribution due to crosstalk that can affect parameters such as dynamic range and fixed pattern noise. So, depending on the features added to the architecture and the technology available, photodiodes may not be a good choice for image sensor arrays.

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