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3-layered Capacitive Structure Design for MEMS Inertial Sensing

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Abstract – In this paper a two-terminal capacitive structure is presented in which a novel architecture with a double interleaved (interdigitated) scheme is introduced. This structure was originally conceived as a mechanism to achieve a greater capacitance between the plates (terminals) of an integrated capacitor using a relatively smaller design area in the standard 0.5µm, two polysilicon and three metal layers (2P3M) CMOS technology. This work presents the design and theoretical analysis of a three-metal interleaved structure used as a varactor tied down to the proof mass of an integrated CMOS-MEMS accelerometer where the active devices are floating-gate transistors (FGMOS) with a variable capacitive coupling coefficient. Nevertheless, the three-layered geometrical scheme may have a wide range of applications across the MEMS technology.

Keywords – CMOS-MEMS, floating-gate, capacitive sensing, capacitive MEMS, FGMOS, COMSOL.

I. INTRODUCTION

The standard CMOS process technology provides VLSI designers with many ways to produce high quality capacitors integrated within the polysilicon and metal fabrication layers. The most popular of these techniques is the one involving a plate of Poly 2 over a layer of Poly 1, separated by a 40nm thickness SiO_2 layer [1]. Although different technologies (all of them named after their minimum feature size) have different number of available metal layers, the 0.5µm fabrication process (2-Poly 3-Metal) from On Semiconductor, in which the minimum channel length is 0.6µm, is proven to be sufficient and reliable to develop CMOS-MEMS devices, specially, those were a metallic proof mass acts as a capacitive transducer.

In [2], [3] and [4], many capacitive structures for inertial measurement devices have been described. They differ from some many other works by taking advantage of two out of the three metal layers available with the 0.5µm CMOS process to build spring-supported capacitive-coupling MEMS circuits, instead of having the MEMS-dedicated technology chip and the CMOS signal processing circuit separately as an hybrid presentation. In this work we show the advantages and drawbacks of a 3-layer interdigitated structure, all integrated within a single CMOS silicon die as well.

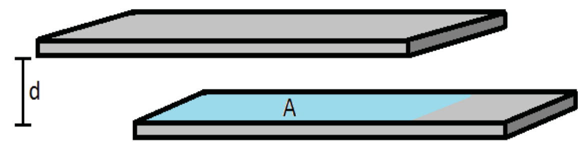

Fig. 1. Geometric parameters of a parallel plates capacitor.

In advance to an upcoming fabrication process and characterization, the goal in this paper is mainly to analyze the viability and estimate the performance of the proposed capacitive structure with basis in a comparative between a few interdigitated and full plate capacitor alternative schemes.

This design might be included as part of the test mobile mass in both accelerometer and gyroscope devices within an integrated CMOS inertial measurement unit (IMU), where capacitive structures are usually used as transducer element.

For that purpose, we set our start point from the simplest expression (eq. 1) for the capacitance between two parallel conductor plates (Fig. 1):

$$C = \frac{\epsilon_0 A}{d} \tag{1}$$

where ϵ_0 is the electric permittivity of free space, A is the overlap area between the two plates and d is the separation gap.

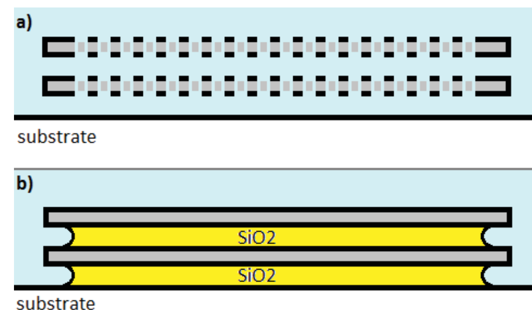

Fig. 2. a) perforated structure (totally released) b) full plate structure (with remaining silicon dioxide).

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For a typical analysis we consider the relative permittivity of the air (all around the structure) equal to 1. And in the particular case of a $0.5\mu m$ process chip, we refer the distance from Metal 1 layer to Metal 2 layer and from Metal 2 to Metal 3 to be $1.1\mu m$ as seen on [1].

It is important to notice that the electronic and electric devices in a standard CMOS fabricated chip are embedded within multiple layers of SiO_2 with a thick top passivation of silicon nitride so, it is needed to place overglass-through windows where a silicon dioxide etchant may release the movable structures. Hence, the dielectric of the capacitive structures will now be air instead of silicon dioxide and the analysis is made in these conditions.

Another issue related to the etching process is the need to include narrow or perforated structures all over the proof mass so the etchant could find its way underneath. A single non-perforated plate might prevent SiO_2 from being totally removed by the etchant beneath the plate (Fig. 2). This is why an interdigitated structure is selected instead of a full plate capacitor structure.

II. THEORETICAL CONCEPTS

First, the capacitor unit to be studied is defined either as the one formed by two “fingers” one above another (different metal layers) or side by side (same metal layer). In agreement with the design rules provided in [5] there are some minimum distances to be established between two adjacent metal wires on chip, this is the case of d_{fin} which is the distance between two fingers in the same layer and d_{tip} corresponding to the gap separation from the tip of a finger and the plate in front of it. It is also defined W_f as the width of the finger and L_f as the length of the part of the finger which overlaps a finger in another layer, so the area A of a layer-to-layer capacitor unit is W_f times L_f. Fig. 3 shows the geometrical attributes of a so called finger as well as Fig. 4 describes how a multi-finger array fits the area available for the capacitive structure in all the three metal layers (ultimately one above the other).

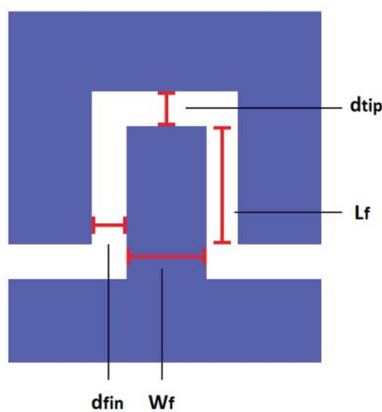

Fig. 3. Geometrical parameters of a finger plate.

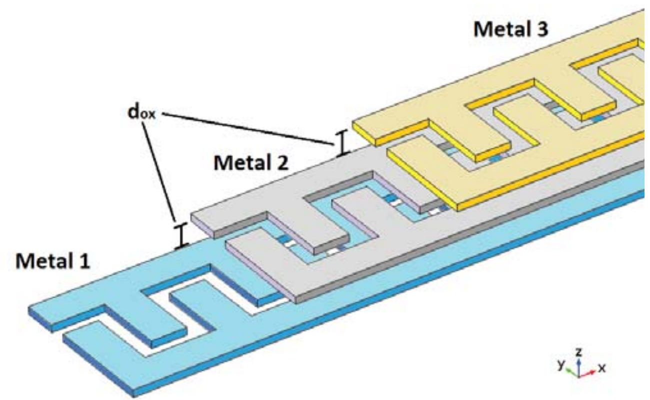

Fig. 4. Interdigitated finger array in the different metal layers for the available design area. Metal 2 fingers partially overlap Metal 1 fingers and so do Metal 3 fingers over the Metal 2 ones.

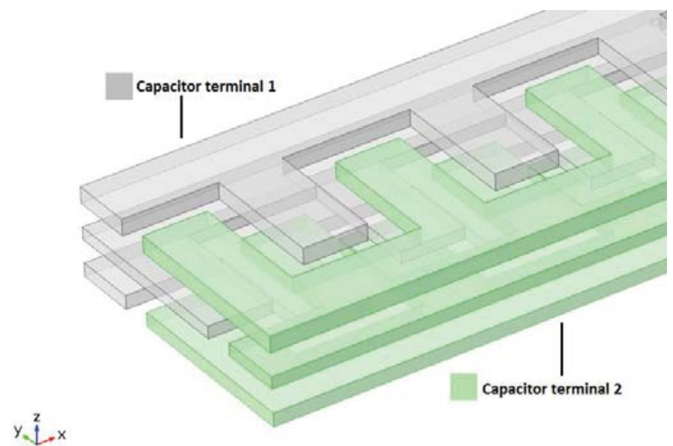

Fig. 5. 3D Rendering for the capacitive structure.

The total capacitance is also intended to consider two other capacitor units, one of them given by a finger and another next to the first in the same layer but tied to a different electric terminal (the other one) so the capacitor area is L_f times t_M, the thickness of the layer. The third capacitor unit corresponds to the tip of a finger and the plate in front of it with a capacitor area of W_f times t_M.

We may recall from [1] the thicknesses of each metal layer as $t_{M1} = 0.64\mu m$, $t_{M2} = 0.57\mu m$ and $t_{M3} = 0.77\mu m$. All the three layers separated uniformly by a $1.1\mu m$ gap, now depicted as d_{ox}. Fig. 5 shows a 3D approach to the multi-layer structure.

Finally, according to the functioning principles of an inertial measurement sensor, we look for the variation in the capacitance due to a displacement of the proof mass.

Since one of the terminals of the capacitor is anchored to substrate and the other one is tied to the movable mass we define y as the mass displacement from its steady position.

The capacitance of the structure (with n fingers) at any given displacement (from $-0.6\mu m$ to $0.6\mu m$ in this design) is:

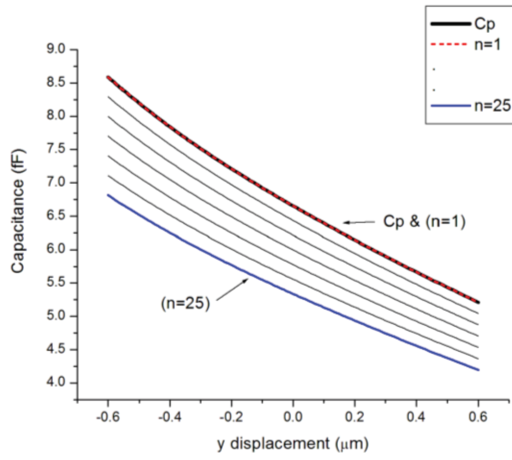

Fig. 6. Capacitance for structures with 1 to 25 fingers.

$$C_y = \frac{2 \cdot n \cdot \epsilon_0 \cdot W_f \cdot (L_f - y)}{d_{ox}} + \frac{(n-1) \cdot \epsilon_0 \cdot (t_{M1} + t_{M2} + t_{M3}) \cdot (L_f - y)}{d_{fin}} + \frac{n \cdot \epsilon_0 \cdot W_f \cdot (t_{M1} + t_{M2} + t_{M3})}{d_{tip} + y} \quad (2)$$

It is important to compare this multi-finger structure with its single-plate counterpart from which capacitance is given by:

$$C_{plate} = \frac{2 \cdot \epsilon_0 \cdot W_{plate} \cdot \left(L_{plate} - x\right)}{d_{ox}} + \frac{\epsilon_0 \cdot W_{plate} \cdot (t_{M1} + t_{M2} + t_{M3})}{d_{tip} + x} \quad (3)$$

Fig. 6 shows a comparison between the single-plate structure and the ones corresponding to 1 to 25 fingers. The width of the fingers for this simulation is dynamically adjusted considering a minimum d_{fin} separation between them and as might be inferred, a one finger capacitor (covering the available area) and the full plate have the same effect.

III. METHODS AND SIMULATIONS

Having a single plate (or the wider finger possible) might be considered as the highest capacitance scenario, yet discarded since the etching criteria seen before takes more relevance. This is why this work proceeds with a comparison between multi-fingered structures.

As we have seen, the proposed structure has interleaved fingers in both x-axis and z-axis (Fig. 5) from the point of view of electric terminals. Nevertheless we may consider the case of having a mass displacement along the y-axis but the finger interleaving only in the x-axis where every finger above or below one another is part of the same terminal as seen in [2] [figure 4] differing from the double interleaved capacitance C_y, for this case and extended for three layers the total capacitance would be given by:

$$C_{fin(y)} = \frac{(n-1) \cdot \epsilon_0 \cdot (t_{M1} + t_{M2} + t_{M3}) \cdot (L_f - y)}{d_{fin}} + \frac{n \cdot \epsilon_0 \cdot W_f \cdot (t_{M1} + t_{M2} + t_{M3})}{d_{tip} + y} \quad (4)$$

Furthermore, proof mass may also have its main displacement in x-axis, what may lead to a finger getting closer to another one and away from the one in the other side with a total capacitance:

$$C_{fin(odd)} = \left(\frac{n-1}{2}\right) \cdot \frac{(2d) \cdot \epsilon_0 \cdot (t_{M1} + t_{M2} + t_{M3}) \cdot (L_f - x)}{{d_{fin}}^2 - x^2} + \frac{n \cdot \epsilon_0 \cdot W_f \cdot (t_{M1} + t_{M2} + t_{M3})}{d_{tip}} \quad (5)$$

when having an odd number n of fingers, and

$$C_{fin(even)} = \left(\frac{n}{2} - 1\right) \cdot \frac{\epsilon_0 \cdot (t_{M1} + t_{M2} + t_{M3}) \cdot (L_f)}{d_{fin} + x} + \left(\frac{n}{2}\right) \cdot \frac{\epsilon_0 \cdot (t_{M1} + t_{M2} + t_{M3}) \cdot (L_f)}{d_{fin} - x} + \frac{n \cdot \epsilon_0 \cdot W_f \cdot (t_{M1} + t_{M2} + t_{M3})}{d_{tip}} \quad (6)$$

otherwise. Fig. 7 describes how different are the five cases according to their electric terminal distribution and displacement orientation.

Finally, Fig. 8 shows an electromechanical simulation via the suite of COMSOL Multiphysics© in which platform a capacitance vs displacement simulation is performed for the 25-finger structure rendered in Fig. 5. The simulation reveals a behavior similar in magnitude to the predicted for C_y in equation 2 and shown in Fig. 7 but also considering not only the plate to plate effects from equation (2), but also parasitic non-parallel-plate capacitances.

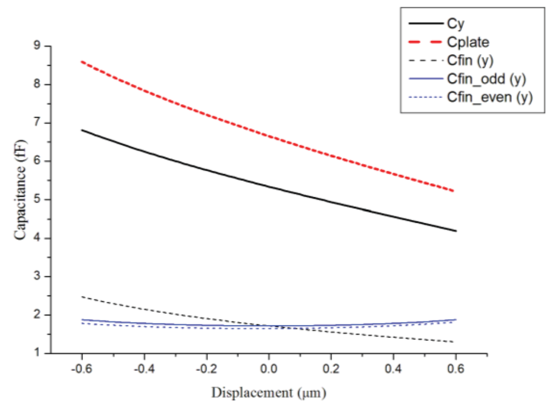

Figure 7. Capacitance differences among the five analyzed cases.

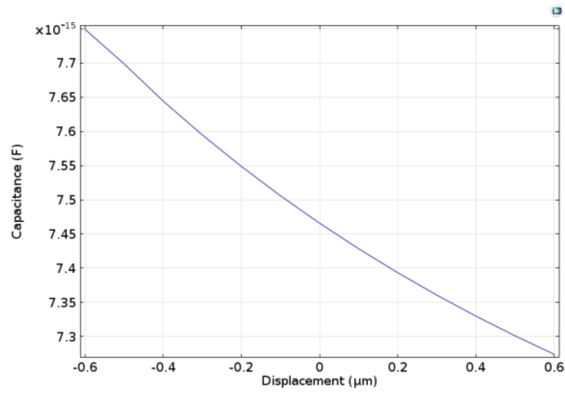

Fig. 8. Physical simulation in agreement with simplified model predictions.

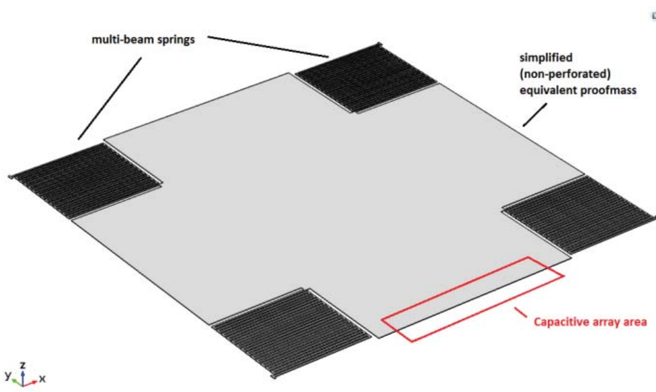

Fig. 9. Equivalent proof mass and springs designed for the inertial measurement unit.

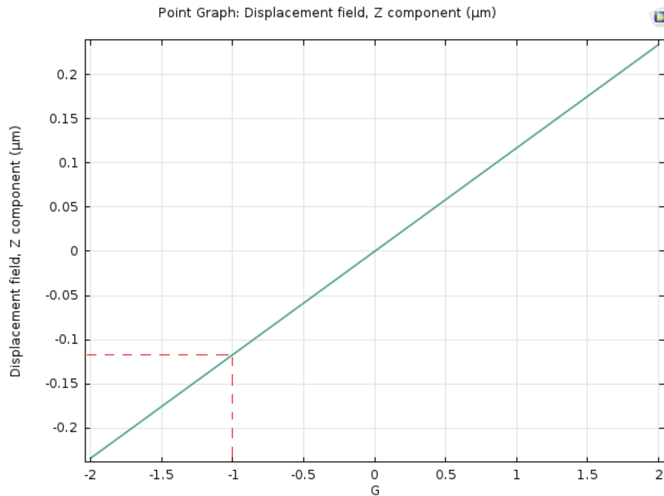

Fig. 10. Prescribed displacement at 1G downwards (gravity acceleration).

By physical simulation, we can also add the effect of gravity acceleration to the proof mass-spring structure, resulting in a prescribed displacement in direction –z due to the weight of the proof mass.

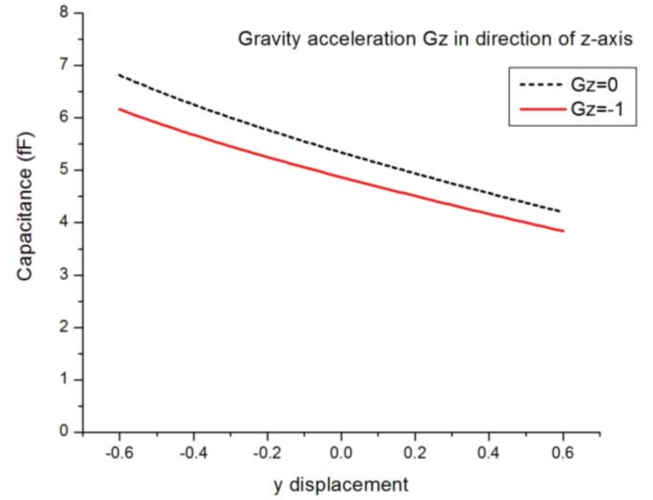

Fig. 11. Total capacitance with and without the effects of gravity.

Fig. 9 represents the spring mass system actually designed to be used within an inertial measurement unit. The capacitive structure subject of this work might be placed in one or more edges of the proof mass, according to the electric circuit used to sense the capacitance variation if this circuit is either differential or not.

The simulation result (Fig. 10) including gravity acceleration at 1G (-ẑ) shows a displacement of about 0.12μm which is a little more than a tenth the air gap between metal layers. This displacement does not have a great effect in the resultant capacitance because as the Metal 2 layer gets closer to Metal 1 gets more separated from Metal 3 as well. Equation 7 includes this displacement and affects the plate-to-plate capacitor unit distance. Fig. 11 is a comparative between the capacitances given by equation (7) and equation (2), this is, with and without the z displacement due to gravity.

$$C_{y,z} = \frac{n \cdot \epsilon_0 \cdot W_f \cdot (L_f - y)}{d_{ox} + z} + \frac{n \cdot \epsilon_0 \cdot W_f \cdot (L_f - y)}{d_{ox} - z} + \frac{(n-1) \cdot \epsilon_0 \cdot (t_{M1} + t_{M2} + t_{M3} - 3z) \cdot (L_f - y)}{d_{fin}} + \frac{n \cdot \epsilon_0 \cdot W_f \cdot (t_{M1} + t_{M2} + t_{M3} - 3z)}{d_{tip} + y} \tag{7}$$

IV. CONCLUSIONS

Being C_y the capacitance variation within the displacement limits fixed by the so designed mass-spring system, we assume a considerable increment in capacitance on behalf of more commonly used techniques such as the ones described in equations (4), (5) and (6). This calculated/simulated effective capacitance is not highly affected by gravity since proof mass is an aluminum thin block about 1×10^{-11}kg and also slightly damped by the air film under it.

This is in agreement with the etching criteria and the CMOS process design rules. Also, due to its fairly linear behavior the structure variable capacitance results suitable for capacitive sensing of inertial phenomena in devices such as accelerometers and gyroscopes.

V. FUTURE WORK

To the date, this design is about to be proved and characterized as it is currently on fabrication process. The structure is intended to interact with CMOS-based floating-gate transistors as a mechanism to obtain a single-chip low-voltage inertial measurement unit.

ACKNOWLEDGMENTS

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