Parasitic Gate Resistance Impact on Triple-Gate FinFET CMOS Inverter

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***Abstract*— In this paper, based on a full intrinsic–extrinsic model for symmetric doped double-gate MOSFET, we analyze the impact of FinFET gate resistance over the inverter and ring oscillator performance. It is shown that, when the total number of fins remains constant, the propagation delay can be improved thanks to the multifinger configuration that translates into the gate resistance reduction. Furthermore, the fin spacing in addition to source/drain fin extension reduction are of primary importance to improve the digital circuit performance.**

***Index Terms*— CMOS inverter, CMOS ring oscillator (RO), digital circuits, FinFETs, high-speed performance, parasitics.**

I. Introduction

CMOS technology has progressed astonishingly in these last decades due to the successful shrinkage of the transistor size, which has been described along the years by Moore's law [1], [2]. The CMOS inverter is considered as a major digital building block and the ring oscillator (RO) is used for benchmarking the technology performance for digital applications [3], [4]. Nonetheless, the traditional design methodologies used by the community for digital electronics neglect the extrinsic gate resistance ($R_{\rm ge}$) [5]. Moreover, some authors have indicated the necessity to reduce the transistor gate resistance in order to get high-speed deep-submicron CMOS circuits [6]–[8]. In this regard, as the CMOS technology goes toward the nanometer range, the gate electrode geometry is reduced in order to get fabrication viability, which can produce an important increment in the electrode sheet resistance and hence $R_{\rm ge}$ increase [6], [8].

On the other hand, triple-gate FinFET (TG-FinFET) technology has emerged as the suitable technology to pursue the more-Moore roadmap thanks to their superior immunity against short-channel effects (SCEs). However, it has been demonstrated that TG-FinFETs exhibit high parasitic series ($R_{\rm sd} = R_{\rm se} + R_{\rm de}$) and gate ($R_{\rm ge}$) resistances as well as gate capacitances ($C_{\rm gge} = C_{\rm gde} + C_{\rm gse}$), caused by their 3-D nature [9], [10]. These parasitics lead to strong deleterious effects over the device high-speed and RF performance [11]–[16].

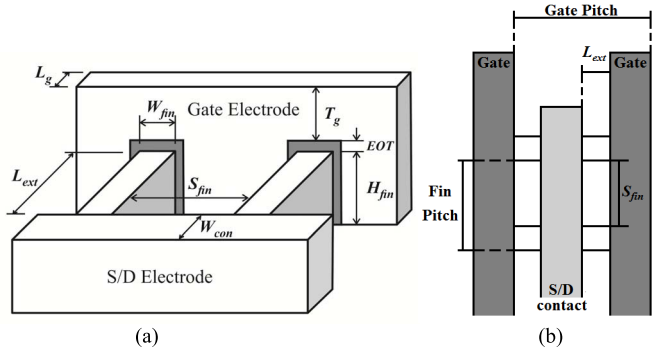

Fig. 1. Schematic of the TG-FinFET. (a) Main geometrical parameters are shown [35]. (b) Top view showing the fin and gate pitch.

In this context, the adequate analysis of the $R_{\rm ge}$ impact over the digital circuit performance, as well as the proper design strategies including $R_{\rm ge}$ and the transistor geometry are of first importance in order to pursue the FinFET technology toward the nanometer range nodes.

Under this scenario, several works have addressed, from the experimental point of view, the FinFET features of digital [17]–[20], analog [21]–[23], and mixed-mode [24], [25] applications, as well as from the process integration [26]–[30] point of view. Additionally, several works focus on the simulation of FinFETs [31]–[34] in order to analyze the digital circuit performance based on inverter and RO.

Tables I and II show the main geometrical dimensions considered in some experimental and simulation works, respectively. Fig. 1(a) and (b) represents those geometrical dimensions [35], where L_g is the channel length, $W_{\rm fin}$ and $H_{\rm fin}$ are the fin width and height, $S_{\rm fin}$ is the spacing between fins, $L_{\rm ext}$ is the distance between the channel and the source/drain electrode, EOT is the equivalent oxide thickness of the gate dielectric, and T_G is the gate electrode thickness. Also, $N_{\rm finger}$ is the number of fingers, $N_{\rm fin}$ is the number of fins

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TABLE I
SUMMARY OF THE TG-FinFETs FEATURES AS DESCRIBED IN [17]–[31]

PARAMETER	REFERENCE													
	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]
L_g (nm)	75	50	35	25	55	40,60,120	40	25	45	24	30	50	20	30
EOT (nm)	1.6-1.9	2	1.5	1.6	2	1.8	1.8	1.1	2.1	---	1.6	2.2	---	0.9
W_{fin} (nm)	30	20	35	10	28	22,32,42	12,22,32	12	17	13	20	20	8	8
H_{fin} (nm)	60	65	60	80	60	60	60	25	60	30	65	55	42	34
T_G (nm)	---	100	---	---	---	100	---	---	100	56	150	---	---	---
L_{ext} (nm)	---	---	---	---	40-100	---	100	10	---		200	---	---	---
S_{fin} (nm)	170	---	175	---	---	328	328	38	---	28	---	100,200	34	52
N_{finger}	---	---	2	---	50,100	50	48	---	1	---	---	----	---	---
N_{fin}	---	---	6	---	12,6,3	6	10	---	5	---	---	----	---	---
N_{tf}	---	14	12	60	300	300	480	---	5	---	---	----	---	---
t_p (ps)	12.5	>9	~ 10	60	---	---	---	---	---	---	---	----	---	---

TABLE II
SUMMARY OF THE THEORETICAL TG-FinFETs FEATURES FOR DIGITAL APPLICATIONS AS DESCRIBED IN [31]–[34]

PARAMETER	REFERENCE			
	[31]	[32]	[33]	[34]
L_g (nm)	16-32	25	14	14
EOT (nm)	1.2	1.0	0.72	1.0
W_{fin} (nm)	8	10	9.4	7
H_{fin} (nm)	16	40	20	19
N_{tf}	---	---	---	6
t_p (ps)	---	~ 5.5	~ 4	>5

controlled by each finger, $N_{\rm tf}$ is the total number of fins ($N_{\rm tf} = N_{\rm finger} \cdot N_{\rm fin}$), and t_p is the RO propagation delay.

As can be observed from Tables I and II, the main geometrical features are spread over a pretty wide range of values, which implies a lack of clear guidelines for FinFETs optimization for digital applications. It is worth to note that L_g is restricted by the technology; also, $W_{\rm fin}$ and $H_{\rm fin}$ are limited by the control of the SCE, and hence they can only be varied in a narrow range. On the contrary, the transistor intrinsic behavior is independent of $S_{\rm fin}$, $L_{\rm ext}$, and T_G, whereas the parasitic parameters are strongly dependent on them. Thus, the overall device performance is, indeed, affected by the parasitics and thus by $S_{\rm fin}$, $L_{\rm ext}$, and T_G.

In this paper, a full intrinsic–extrinsic model for symmetric doped double-gate MOSFET (SDDGM) [9] together with geometry-dependent parasitic models [35]–[37] have been implemented in Verilog-A with the aim to perform circuital SPICE simulations of both n- and p-type transistors. Several models for the parasitic series resistances and capacitances, which can consider additional components have been presented [38]–[42], however, in some cases the dependences with the geometrical fin parameters are ignored or they are not properly validated from the experimental point of view.

Therefore, a CMOS inverter and a three-stage RO have been simulated. Finally, the impact of the gate extrinsic resistance over the circuit performance and the guidelines for the geometry tuning have been analyzed.

II. MODEL IMPLEMENTATION

Very recently, it has been demonstrated that the intrinsic–extrinsic SDDGM [9] models well the dc and RF measured performance of n-type TG-FinFETs. The intrinsic part of the model is valid below and above the threshold as well as in linear and saturation conditions. Furthermore, it includes SCEs and the field-dependent mobility model [43]. This model was originally developed for double-gate MOSFETs, however, it has shown to be able to reproduce the FinFET behavior [44]–[47]. Also, for TG-FinFETs, the relative weight of the lateral channels is very high with respect to the top one, thus the SDDGM model properly reproduces their characteristics [44]–[47]. Furthermore, the intrinsic capacitances have been added [47]. The model requires only a few fitting parameters to accurately reproduce the transistor behavior [43], while other available models require a large number of fitting parameters [48]. The capability of the SDDGM model to perform analog circuit simulations is shown in [49].

As was shown previously, several experimental parameters, such as: 1) transfer and output dc characteristics; 2) extrinsic transconductance (g_m) and output conductance (g_d); 3) intrinsic small-signal equivalent circuit parameters ($g_{\rm mi}$, $g_{\rm di}$, $C_{\rm gdi}$, $C_{\rm gsi}$); 4) extrinsic small-signal equivalent circuit parameters ($R_{\rm se}$, $R_{\rm de}$, $R_{\rm ge}$, $C_{\rm gde}$, $C_{\rm gse}$); 5) two-port behavior (Z- and Y-parameters); and 6) cutoff frequencies, have been properly described [9].

The full intrinsic–extrinsic model has been implemented in Verilog-A. The parasitic parameters are included in the intrinsic device as lumped elements, which have been calculated for multifin-multifinger configuration as shown in [9]. It is worth to note that the parasitic models have been validated by comparison with experimental measurements in a wide range of geometries [9]. This intrinsic–extrinsic model constitutes a circuit basic cell that has been used for the SPICE implementation of both n- and p-type transistors. Fig. 2 shows the comparison of the experimental and modeled transfer characteristics for a 40-nm n-type FinFET, and in the inset of Fig. 2, a comparison between the experimental and modeled output characteristics and the basic cell used [9] are shown.

Afterward, a CMOS inverter and a three-stage RO were implemented using a SPICE simulator, as shown in Fig. 3(a) and (b). Multifin-multifinger configurations are considered for both n- and p-type transistors and the total number of fins is fixed to 12 and 24, respectively.

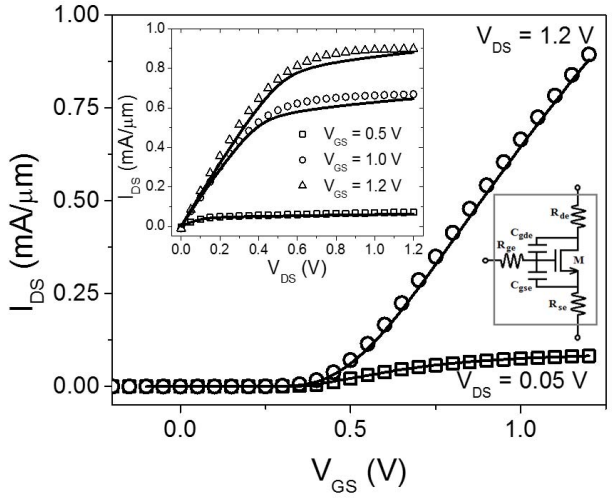


Fig. 2. Comparison of the experimental and modeled transfer characteristics. Inset: the comparison of the experimental and modeled output characteristics and the basic cell used for SPICE simulation.

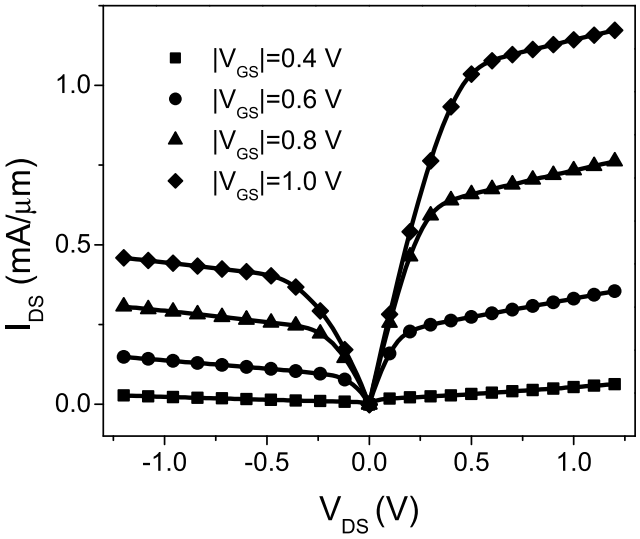


Fig. 4. Output characteristic of the 22-nm channel length n- and p-type FinFET. The main geometrical dimensions are: $L_g = 22$ nm, $W_{\text{fin}} = 10$ nm, $H_{\text{fin}} = 60$ nm, EOT = 1.4 nm, $S_{\text{fin}} = 50$ nm, $L_{\text{ext}} = 50$ nm, and $T_G = 50$ nm.

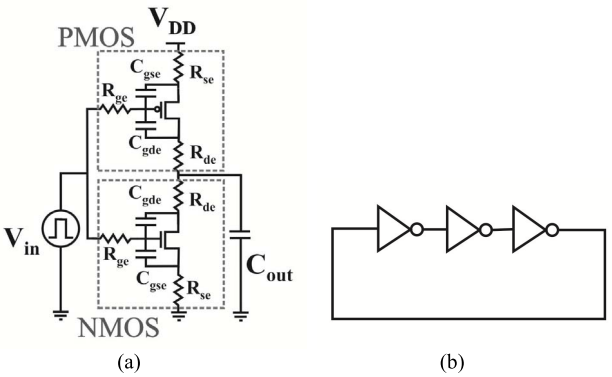


Fig. 3. (a) CMOS inverter and (b) RO implemented in SPICE simulator.

TABLE III
SUMMARY OF THE TG-FinFET PARASITICS

CONFIGURATION	*Transistor Type*	N_{finger}	N_{fin}	Parasitics		
				R_{sd} [Ω]	R_{ge} [Ω]	C_{gge} [fF]
(i)	n	1	12	64	520	0.83
	p	1	24	32	963	1.66
(ii)	n	2	6	64	160	0.83
	p	2	12	32	260	1.66
(iii)	n	3	4	64	91	0.83
	p	3	8	32	127	1.66

Fig. 4 shows the width normalized output characteristics for both n- and p-type transistors, with a 22-nm channel length and W_{fin} and H_{fin} of 10 and 60 nm, respectively. The electron mobility in the n-type transistor is considered as twofold of the hole mobility of the p-type transistor, as was experimentally observed in [19].

In order to analyze the impact of R_{ge} over the circuit performance, N_{finger} and N_{fin} will be varied, but always maintaining N_{tf} constant. It is worth to note that when the total number of fins is fixed, the total transistor width remains constant and thus the intrinsic device and the parasitic R_{se}, R_{de}, and C_{gge} are considered constant [9], [35], [36]. On the contrary, R_{ge} is dependent on both N_{fin} and N_{finger} [9], [37].

III. PARASITIC GATE RESISTANCE IMPACT OVER CMOS INVERTER

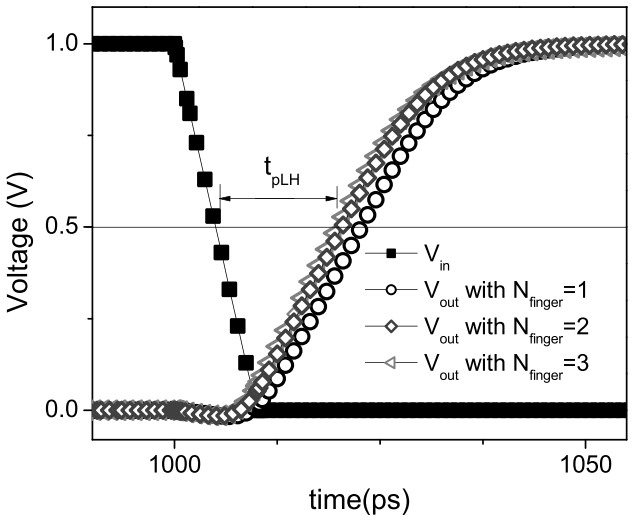
A CMOS inverter was simulated considering the 22-nm node, with W_{fin}, H_{fin}, S_{fin}, and L_{ext} of 10, 60, 50, and 50 nm, respectively. The gate stack corresponds to an EOT of 1.4 nm and a T_G of 50 nm. An output capacitance (C_{out}) is considered as the parallel arrangement of the total gate capacitance of both n- and p-type transistors [5]. Thus, it is possible to consider the output capacitance as

$$C_{\text{out}} = C_{\text{ggen}} + C_{\text{ggin}} + C_{\text{ggep}} + C_{\text{ggip}} \tag{1}$$

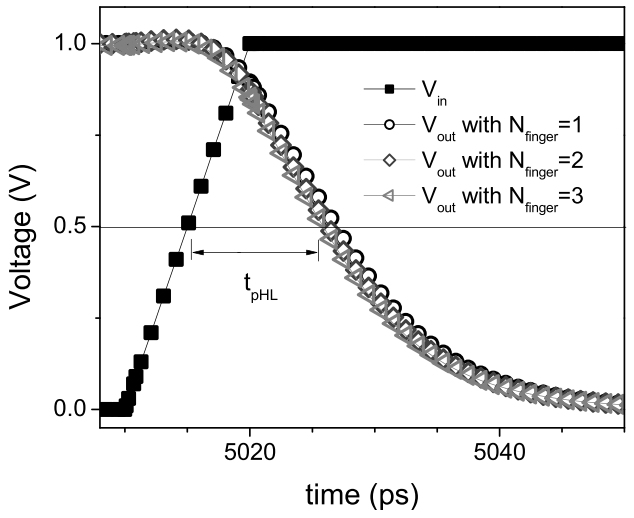
where C_{ggen} and C_{ggep} are the parasitic total gate capacitances for the n- and p-type FinFETs, respectively, while C_{ggin} and C_{ggip} are the intrinsic gate capacitances. In the case of the FinFET transistors, C_{gge} becomes even greater than the intrinsic counterpart [10], for this reason the output capacitance could be very high.

Fig. 5(a) and (b) shows the comparison of the input and output signals when the input goes from high-to-low and low-to-high logic levels, respectively. Three different configurations are considered (Table III): 1) one finger with 12 (n-type) and 24 (p-type) fins per finger; 2) two fingers with 6 and 12 fins per finger; and 3) three fingers with 4 and 8 fins per finger. In this way for all cases the total number of fins is constant to 12 and 24, respectively, for the n- and p-type transistors.

Fig. 5(a) clearly shows that the propagation delay when the output goes from low-to-high (t_{pLH}) is improved as N_{finger} is increased; it passes from about 17.7 to 14.87 ps when the number of fingers changes from 1 to 3, this result implies an improvement of ∼16%.



(a)



(b)

Fig. 5. Comparison of the input and output signals of the 22-nm inverter based on TG-FinFET. The main geometrical dimensions are: $L_g = 22$ nm, $W_{\text{fin}} = 10$ nm, $H_{\text{fin}} = 60$ nm, EOT $= 1.4$ nm, $S_{\text{fin}} = 50$ nm, $L_{\text{ext}} = 50$ nm, $T_G = 50$ nm, and FO $= 4$.

On the other hand, Fig. 5(b) shows that the propagation delay when the output goes from high-to-low (t_{pHL}) exhibits a weaker dependence. It passes from 11.9 to 10.87 ps, which means an improvement of ∼9%. Furthermore, the propagation delay (t_p) measured as the mean value of t_{pLH} and t_{pLH} has an overall improvement of ∼15%.

The impact of R_{ge} on the propagation delay can be analyzed from Fig. 3(a). As can be seen, an *RC* network composed of R_{ge}, R_{de}, and C_{gde} of both p- and n-type transistors is produced. Such an *RC* network is connected between the input and output and it will be activated only for the duration of the transient response. Thus, the propagation delay will be affected. Additionally, for t_{pLH}, the output capacitance will be charged through the p-type transistor because being a wider transistor, the impact of the *RC* network is more important. On the other hand, for t_{pHL}, the output capacitance is discharged through the n-type transistor and hence the

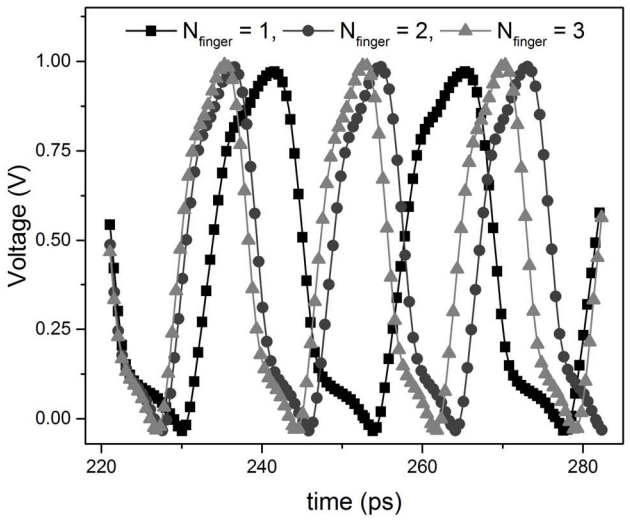


Fig. 6. Output signals of the 22-nm RO based on TG-FinFET. The main geometrical dimensions are: $L_g = 22$ nm, $W_{\text{fin}} = 10$ nm, $H_{\text{fin}} = 60$ nm, EOT $= 1.4$ nm, $S_{\text{fin}} = 50$ nm, $L_{\text{ext}} = 50$ nm, and $T_G = 50$ nm.

RC network impact is reduced. When the devices have two or more fingers, they are connected in parallel and the resistances produced by each one will appear in parallel. Consequently, the total R_{ge} is reduced by use of the multifinger structure [9], [37]. Table III gives a summary of the modeled parasitics for the three configurations.

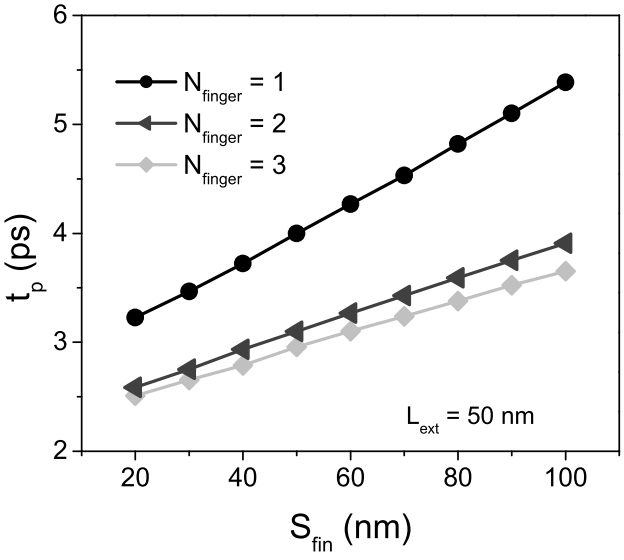
IV. Parasitic Gate Resistance Impact Over Ring Oscillator

An RO was simulated, considering L_g of 22 nm for the three configurations previously described. As was mentioned above, C_{out} is related to the intrinsic capacitances, which are bias dependent. For this reason the use of an RO allows to evaluate the inverter performance, since each inverter becomes the load of the previous stage. In this way, the load capacitance corresponds to a dynamic capacitance.

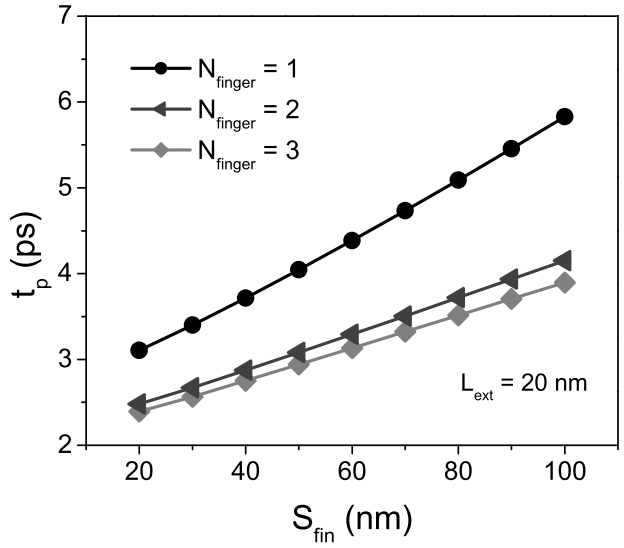
Fig. 6 shows the output signals for the three simulated ROs. As can be seen, the increment on N_{finger} produces a reduction of the propagation delay and thus an increment on the oscillation frequency. Frequency values of 41.9, 54.6, and 57.5 GHz, for N_{finger} equal to 1, 2, and 3, respectively, were obtained. Thus, the RO exhibits an output frequency increment of about 30% and 37% if N_{finger} is increased from 1 to 2 and from 1 to 3, respectively.

Fig. 7(a) and (b) shows the plot of the t_p versus S_{fin} for the three different values of N_{finger} and two different values of L_{ext}. S_{fin} was varied from 20 to 100 nm, which implies a fin pitch from 30 to 110 nm as expected for nanometric nodes [29], [30], [50]–[52], in order to analyze its impact on the inverter performance.

As can be observed, the delay has a strong dependence with S_{fin}, because of the reduction of both C_{gge} and R_{ge} [9]. This indicates that the S_{fin} reduction becomes necessary with the aim to improve the inverter performance. Besides, for large values of S_{fin}, t_p shows a marked reduction (around 27%–30%) with the increment of N_{finger},



(a)



(b)

Fig. 7. Propagation delay versus S_{fin} for oscillators with 1, 2, and 3 fingers and L_{ext} of (a) 50 and (b) 20 nm. The main geometrical dimensions are: $L_g = 22$ nm, $W_{\text{fin}} = 10$ nm, $H_{\text{fin}} = 60$ nm, EOT = 1.4 nm, and $T_G = 50$ nm.

from 1 to 2 at both L_{ext} conditions. R_{ge} decreases as S_{fin} is reduced, which implies the RO improvement, consequently, when S_{fin} is large the change in N_{finger} implies an important reduction of R_{ge} and thus a delay improvement. Once S_{fin} is reduced, the dependence of N_{finger} over t_p becomes weaker. Nonetheless, the reduction of t_p when N_{finger} passes from 1 to 2 is about 19%–20%, for S_{fin} as narrow as 20 nm in both values of L_{ext}. If S_{fin} is extremely reduced, R_{ge} becomes small and thus the delay improvement due to the increment of N_{finger} is relatively small. Additionally, from the comparison of both the figures, it can be observed that L_{ext} has a weak impact on the RO behavior for S_{fin} values smaller than ~50 nm.

These results clearly show that R_{ge} has an important impact on the inverter behavior, thus it is necessary to use the multifin-multifinger configuration in order to improve the

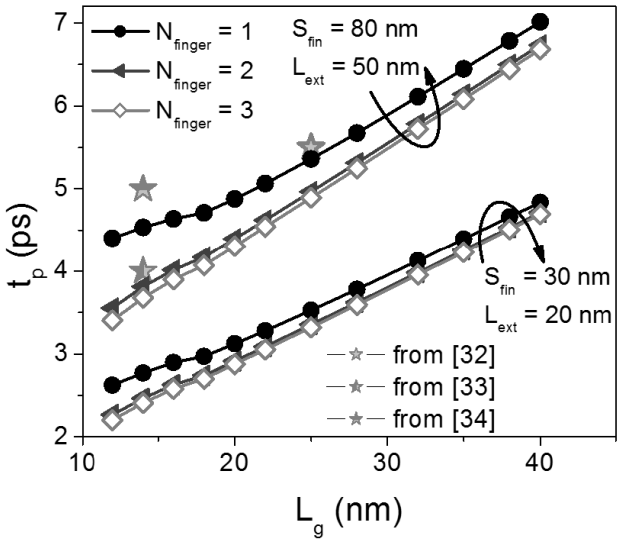


Fig. 8. Propagation delay versus L_g for oscillators with 1, 2, and 3 fingers and $S_{\text{fin}}/L_{\text{ext}}$ of 80/50 nm and 30/20 nm. The main geometrical dimensions are: $W_{\text{fin}} = 4$ nm, $H_{\text{fin}} = 24$ nm, EOT = 1.0 nm, and $T_G = 50$ nm.

circuit performance. Additionally, the reduction of S_{fin} down to 30 nm or the fin pitch down to 40 nm, as well as the minimization of the L_{ext} through the gate pitch below 90 nm can lead to the reduction of the propagation delay down to 3 ps for a 22-nm channel length.

V. Ring Oscillator Projection Toward 12 nm Physical Length

Nowadays, novel technologies have been developed with the aim to pursue the CMOS technology toward nanometric nodes. Among others, the gate-all-around FETs (GAA-FETs) as well as the silicon nanowire FETs (SNW-FETs) appear as promising alternatives for sub-20 nm [53]–[55]. However, the FinFET feasibility for nanometric nodes was demonstrated thanks to the development of a 10-nm platform [30]. Under this scenario, due to the reduced geometry, these technologies will suffer from a high parasitic R_{ge} and hence it is necessary to analyze its impact over the circuit performance.

Therefore, based on the model, RO with different channel lengths from 40 to 12 nm were simulated, with the objective to show a theoretical trend of the R_{ge} impact over the FinFET circuit performance as the channel length is reduced toward the nanometric range. W_{fin} was fixed to 4 nm in order to keep the fin length/width ratio to 3, for the smallest L_g, with the aim to reduce the SCE [56], [57]. H_{fin} is fixed to 24 nm and the gate stack considers a dielectric layer with EOT of 1 nm and the thickness of the gate electrode of 50 nm.

Fig. 8 shows the propagation delay versus the channel length for S_{fin} and L_{ext} with values of 80 and 50 nm, as well as 30 and 20 nm. The three $N_{\text{finger}} - N_{\text{fin}}$ configurations are shown.

As can be seen, the difference in t_p between one and two fingers becomes more important as L_g is reduced. This implies that for relatively long transistor technologies the

impact of R_{ge} can be negligible, however, for nanometer range nodes it cannot be neglected any longer.

Additionally, the single-finger RO has a strong degradation for L_g smaller than 20 nm, since the t_p reduction is weaker than for a 20–40 nm channel length. On the other hand, as N_{finger} increases the delay is improved and the same reduction trend is observed in the full L_g range. Moreover, the minimum delay achieved is ∼3.5 ps for 12-nm devices, which is comparable with the theoretical reports for sub-32-nm technology nodes [32]–[34].

In addition, the reduction of S_{fin} and L_{ext} produces a noticeable improvement in the RO performance with a delay that can be reduced down to 2.6 ps for a 12-nm single-finger RO. Besides, for the two-finger case, a small reduction of t_p (11%) is still observed to levels down to 2.3 ps for a 12-nm node, which is even smaller than the theoretical reported values [32]–[34]. Moreover, this reduction implies a frequency increment of about 20%, which is significant. Furthermore, as the channel length is reduced to below 20 nm, the gate metal layer sheet resistance can increase significantly as indicated in [6], therefore, the simulation results presented in this paper will underestimate the R_{ge} impact for nanometric technology nodes. In this scenario, the multifinger consideration becomes even more important in order to reduce the total gate resistance.

Finally, as the channel length reaches 12 nm, the gate resistance will be more and more important, due to the increment of the metal gate sheet resistance as well as the necessity of extremely reduced device geometry. This fact will affect the FinFET technology, but also different kinds of technologies such as GAA-FETs, SNW-FETs, or MuGFETs. Hence, for the near future technologies it will be necessary to include the parasitic gate resistance and the multifinger configuration in order to develop adequate circuit design and optimization strategies.

VI. Conclusion

A CMOS inverter and an RO based on TG-FinFETs have been simulated. The impact of the gate extrinsic resistance has been investigated by a comparison between the performance of single-finger and multifinger configured circuits. The overall results indicate that the circuit performance is strongly affected by the parasitic gate resistance. The impact of R_{ge} over the inverter and the RO behavior has been demonstrated, as well as the necessity to consider the mutifin-multifinger configuration and the reduction of S_{fin} and L_{ext} in order to improve the digital circuit performance.

Finally, the results indicate the necessity to include R_{ge} in the transistor model in order to develop proper design methodologies for nanometrer range digital circuits based on TG-FinFETs.

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