

Reconfigurable arithmetic logic unit designed with threshold logic gates

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Abstract: In recent years, there is a trend towards the development of reconfigurable circuits where devices using them offer flexibility and performance. Different technologies are explored, such as threshold logic gates (TLGs), which are one of the most promising future technologies, and researchers are examining and improving different characteristics such as density, performance and power dissipation. This research presents a 4-bit arithmetic logic unit (ALU), which was designed using TLGs through reconfigurable logic blocks with a universal circuit configured with three stages based on a floating-gate metal oxide semiconductor transistor with more than one control gate, which was named neu-complementary metal oxide semiconductor (ν -CMOS). The main contribution is that this device is configured as a ν -CMOS inverter and has the ability to program the threshold voltage of its transfer curve by applying an external voltage to the additional control gates. The number of input bits and the magnitude of the weighted input capacitances related to control gates of the ν -CMOS inverters is obtained and analyzed by using the graphical method (floating-gate potential diagram). Finally, the proposed 4-bit ALU shows similar results as those measured from the ALUs implemented in the field programmable gate array evaluation kit and the Motorola chip MC14581B.

1 Introduction

Although threshold logic gates (TLGs) have been a research area covered since a long time ago, currently it is now considered that very-large-scale integration (VLSI) implementations are not still mature enough; several approximations for configurations that use capacitive, conductance/current or differential implementations can be found [1]. Also, reconfigurable [2–6] and not reconfigurable developments [7–9] based on TLGs are available.

At present, it is considered that a reliable development of the threshold logic is being delayed since the TLG design is based on the full-custom design methodology and because there is lack of high-level synthesis tools [1, 10]. In general, the utility of TLGs as a design alternative will be determined not only by the availability of feasible basic blocks, costs and performance capacity but mainly by the existence of automated synthesis tools that can improve all its properties. For example, algorithms are being proposed as part of the research generated by the importance of TLG and its potential [11, 12]. In addition, theoretical and experimental efforts from particular advantages are being carried out, which were identified in the use of logical threshold circuits. Although there are still performance limitations, such as the static energy consumption, the fan capacity, the silicon area needed and the dispersion of the technological parameters, it could be anticipated that once these problems are solved, the design of the TLG circuit may be easy. In this way, contributions reported in [9, 13, 14] show proposals that are being executed to reinforce this logic design methodology.

Reconfiguration is an additional property that can be found between different configurations that can be conceived with TLGs. This property can be achieved using the neu-complementary metal oxide semiconductor (ν -CMOS), which can be described as a multiple-input floating-gate (MIFG) metal oxide semiconductor field effect transistor (MOSFET). A MIFG is a circuit with multiple input gates, which are capacitively coupled to an electrically isolated floating gate. Besides, it has behaviour as a biological neuron to which several signals arrive and are processed

to deliver an output based on an activation function. Correspondingly, in the context of the ν -CMOS, a weighted sum of the voltage applied to each of the inputs in the floating gate is performed, controlling the state *ON/OFF* of the metal oxide semiconductor (MOS) transistor depending on the sum of voltage.

Taking advantage of a well-established threshold level of the system, a TLG can be designed; this can lead to a basic circuit configuration that can perform all the Boolean functions based on programmable-bias inverters with external voltages, whose values depend, in particular, on the designed logic gate. A proper design process of the basic TLG configurations can develop reconfigurable circuits simplifying the number of devices used. A significant difference in the construction of logical functions consists of the number of devices used in TLG circuits compared with conventional gates as mentioned in [2].

Although ν -CMOS transistors are devices with high inherent capacitances, they are still an interesting option for reconfigurable circuits. Despite the problems encountered in the development of TLG circuits, this study proposes a design flow of an arithmetic logic unit (ALU) that uses reconfigurable basic blocks with an emphasis on the design process that can result in a digital system based on the ν -CMOS.

This paper is organised as follows. In Section 2, we describe the ν -MOS technology, whereas, in Section 3, we present the floating-gate potential diagram (FPD) on which the design of the proposed ALU is based. In Section 3, the design methodology where a description is given for the basic blocks and the *fcarry* block is presented. The results obtained from the simulation using the proposed TLG ALU, the comparisons, where the ALU is implemented in both a field programmable gate array (FPGA) evaluation board and a commercial chip are given in Section 4. Finally, Section 5 draws the conclusions.

2 ν -MOS technology

The development of circuits began in the 1930s with the creation of the field-effect transistor, passing through the bipolar junction

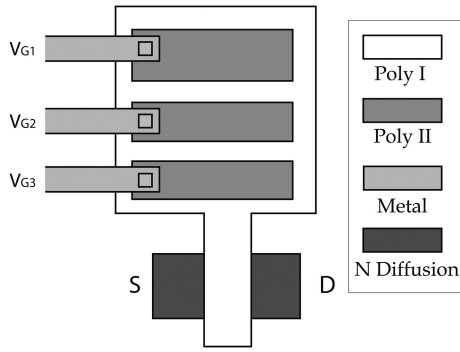


Fig. 1 Topology of a MOS transistor with multiple control gates

transistor (1947), until arriving at the CMOS [P-type MOS (PMOS), N-type MOS (NMOS)], which was designed in 1960 and then used to implement integrated circuits (ICs). The MIFG ν -MOS transistors were developed in 1967 and applied since 1989 in the Electrically Erasable Programmable Read-Only Memory, reducing the number of interconnections on a chip. At the present time, conventional and commercial circuits are still being designed with CMOS, whereas the ν -MOS transistors are used in specific applications. Therefore, the MOSFET transistor is used in the construction of the circuit and can be of type P or N, which results in CMOS technology. This technology allows implementing different passive and active devices, whose dimensions are smaller than square micrometres in the same manufacturing process, and thus integrate them into a small silicon chip. The decision to integrate with CMOS technology is based on the cost and portability of the design.

The trend of memories for neural networks is to use standard technologies such as the 1.2-micron double poly-silicon, which is very accessible. Floating-gate structures report several features such small areas, low power consumption and compatibility with standard technologies. The main challenge of the technology is to reach such scaling, where the area of ICs is optimised, achieving a compromise between the complexity of the circuits and the size of the chip. The floating-gate circuits and conventional MOS circuits have different characteristics. On the one hand, the conventional MOS transistors report: (i) CMOS inverters only have a maximum input for typical use, (ii) circuit arrangements performing a certain function require an area that depends on the number of components (more arrangements involve higher area), (iii) the CMOS inverter requires a small number of capacitances, (iv) the delay times in arrays (to analyse logic gates) have small values, and (v) frequency limits for arrays with these transistors (in logic gates) show high values (above 10 MHz). On the other hand, the reports of the logical ν -MOS present: (i) possibility of implementing multiple control gates such as inputs and feeding one, some or all of the inputs, (ii) advantage of saving transistors in digital circuits, (iii) disadvantage of greater number of capacitances, (iv) the delay times are greater and, consequently, (v) the frequency ranges are smaller.

Fig. 1 shows a double-standard poly-silicon CMOS process, where there are three important points that should be considered when design circuits use ν -MOS transistors: (i) the devices must be discharged with ultraviolet light or other discharge techniques, which remove the residual values stored during manufacturing, (ii) there is a dependence between the drain and source current and the drain voltage of the ν -MOS device, which is more pronounced than in a standard MOSFET and can be minimised using additional techniques (aspect ratios or helmet-type devices), and (iii) the ν -MOS inverter is a standard block of multi-valued binary circuits, where this structure can consume static power depending on the state of the inputs.

The important parameters for the design of the circuits, such as the native threshold voltage and the thickness of the oxide, depend on the used technology. In this case, these parameters occur in two situations: (i) poly-silicon 1 (poly I) and substrate (N-type material), and (ii) poly-silicon 1 (poly I) and poly-silicon 2 (poly II), see Fig. 1. Therefore, it is a primordial requirement to know in advance the respective values of the technology, in order to make

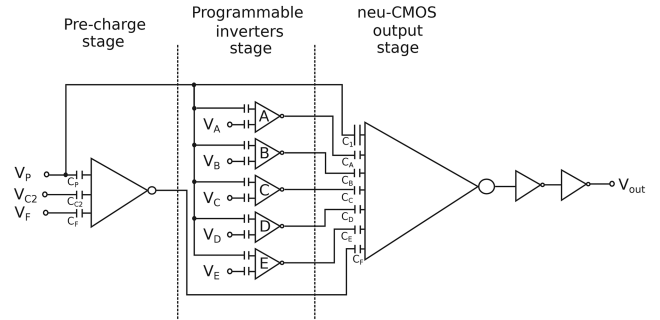


Fig. 2 Block diagram of the basic configuration of a ν -CMOS TLG circuit

the correct computations. In the ALU proposed in this work, the technology is 1.2 μm in length of the channel, double metal, double poly-silicon and well N of AMI, whose parameters are shown in (1), more details in [15]

$$\begin{aligned} V_{th}(n) &= 0.5154122 \text{ V}, \\ V_{th}(p) &= -0.8476404 \text{ V}, \\ \text{tox}(\text{poly II} - \text{poly I}) &= 31.7 \text{ nm}. \end{aligned} \quad (1)$$

Several lines of research in ν -MOS technology are being developed, for example, the work presented in [16] focuses on the loading and unloading times of the ν -MOS transistor, in other words, the injection and extraction of load of the floating gate, as well as the comparisons in power consumption, while in [17], technology that operates with millivolts is reported. In the proposed work, the 4-bit ALU based on TLG uses the 1.2-micron technology and operates at 3.3 V, this is due to the budget allocated for these designs within our institute, and the focus is not on the injection and extraction of load from the floating gate, but the number of transistors used in CMOS and ν -MOS technologies, obtaining significant reduction and high performance.

Mainly, the design based on ν -MOS and TLG presents a drastic reduction in the number of transistors as well as interconnections when it is compared with conventional transistors. For example, a 3-bit A/D converter requires 16 ν -MOS transistors, while requiring 174 conventional CMOS transistors. The reduction in the number of transistors and their interconnections are some of the most studied problems in the design of VLSI logic circuits, for this reason, the floating-gate ν -MOS transistor is a device that reduces the processing time and derives the scalar product in a simple way with the storage of weight in neural networks.

3 Basic configuration and design flow

A ν -CMOS transistor is the core of a TLG circuit and must be designed with several control gates that function as weighted inputs in each stage. Therefore, it is required to know the value of these capacitances to obtain the desired logical function. A graphical representation of each Boolean function can be drawn, where the voltage on the floating gate of the ν -CMOS is plotted as a function of a multi-valued input voltage, named V_P , and mapped from a n -bit digital input.

The authors of [3, 18] showed that the number of programmable inverters, the respective applied external voltage, and the coupling capacitances (weighted) can be derived graphically from the frame called FPD. Logic functions such as AND, NAND, OR, NOR, XOR, and XNOR can be designed using a single basic configuration by applying the respective external voltages, see Fig. 2. The circuit is configured with three basic stages as follows: (a) *pre-charge input* stage consisting of a ν -CMOS inverter with six control gates and a common floating gate; (b) *programmable inverter* stage, which has five programmable ν -CMOS inverters with two control gates each, the latter as inputs, and (c) *output ν -CMOS* stage, where there is a ν -CMOS inverter with ten control gates.

V_P is the multi-valued input that depends on the digital inputs (4 bits) and counts as feeding the three stages. In Fig. 2, V_P represents the input of four bits and is represented by an input to convert it

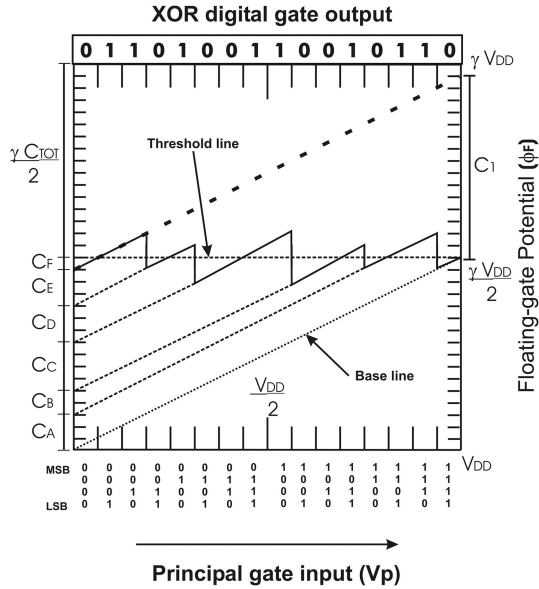


Fig. 3 Theoretical FPD for the output v-CMOS inverter. The case for the XOR gate is illustrated. Values for the coupling capacitances of are $C_1 = (15/32)\gamma C_{TOT}$, $C_A = (3/32)\gamma C_{TOT}$, $C_B = (2/32)\gamma C_{TOT}$, $C_C = (4/32)\gamma C_{TOT}$, $C_D = (3/32)\gamma C_{TOT}$, $C_E = (3/32)\gamma C_{TOT}$, and $C_F = (1/32)\gamma C_{TOT}$

into a multi-valued signal only for simulation purposes. V_{C2} and V_F are used in the first stage to adjust the appropriate output that is required from the pre-charge stage at the time it feeds the v-CMOS inverter in the third stage for a given logic function. The second stage contains five programmable inverters, A, ..., E, and has the purpose of establishing the transition of the respective inverter through the threshold level $\gamma V_{DD}/2$, which is shown in Fig. 3. Finally, C_1, C_A, \dots, C_F representing the weighted inputs that feed the floating gate to trigger on the v-CMOS inverter in the third stage; this is based on the truth table of the corresponding gate.

An XOR gate function is used mainly in the proposed ALU, and Fig. 3 shows the corresponding FPD for the configuration presented in Fig. 2. As a 4-bit input is considered, the x-axis is divided into 16 subdivisions and the y-axis is divided into 32 subdivisions [19]. The threshold level is $\gamma V_{DD}/2$, where γ is the floating-gate gain and is expressed in (2), where C_{TOT} is described in (3); the left y-axis represents the coupling capacitances of the final v-CMOS stage and the right y-axis denotes the voltage range of the floating-gate potential ϕ_{FG} (0 to γV_{DD})

$$\gamma = \frac{C_1 + C_A + C_B + C_C + C_D + C_E + C_F}{C_{TOT}} \quad (2)$$

$$C_{TOT} = C_0 + C_1 + C_A + \dots + C_F \quad (3)$$

To operate properly, some design considerations are described: capacitors C_1 and C_F must be equal in the pre-charge and v-CMOS outputs; also, where C_{ON} and C_{OP} are the gate capacitance of the NMOS and PMOS transistors, respectively; besides, the 4-bit digital input is considered with C_1 , as

$$C_1 = C_{X1} + C_{X2} + C_{X3} + C_{X4} \quad (4)$$

Fig. 2 shows that the 4-bit input feeds the three configuration stages at the same time.

In addition, Fig. 3 shows that the value selected for V_{DD} in this design was 5 V, therefore this will be the maximum value reached by V_P on the x-axis of the FPD for a logical input of '1111'.

The logical output values of an XOR logic gate are represented by the bold solid line, where a logic 1 is presented at the output when $\phi_F > \gamma V_{DD}/2$ and a logic 0 when $\phi_F < \gamma V_{DD}/2$, as specified at the top of the plot. Moreover, by extrapolating each inclined line

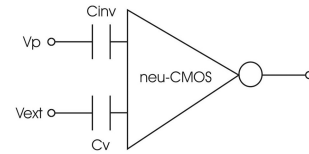


Fig. 4 Block diagram of a programmable inverter; where V_P corresponds to the 4-bit input and V_{ext} is the external voltage input V_A to V_E , corresponding to each used programmable inverter

to the capacitance axis, the magnitude of each coupling capacitance of the v-CMOS, can be derived. The baseline represents the variation of the floating-gate potential of the v-CMOS when the external voltage that feeds all the programmable inverters is zero. Finally, the extrapolation of each vertical line of ϕ_F in Fig. 3 will indicate the external voltage that should be applied to the corresponding programmable inverter (depending on the logic gate considered), either as an absolute voltage value or as a fraction of V_{DD} in general. An FPD can be drawn for different logic gates by means of their corresponding coupling capacitances and external voltage values for the programmable inverters. Moreover, there is no established design standard for the coupling capacitance magnitude in the pre-charge stage, but in this work, it is proposed to follow the usual binary weight for each bit, that is, each input bit is C_0 times the position of bit 2^n , where $n=0, 1, 2, 3$, for the present case. Therefore, $C_{X1} = 2^0 * C_0$, $C_{X2} = 2^1 * C_0$, $C_{X3} = 2^2 * C_0$, and $C_{X4} = 2^3 * C_0$.

Fig. 4 shows a schematic representation of a programmable inverter, where V_P is the multi-valued input given by four weighted input bits represented by C_{INV} , and V_{ext} is the external voltage derived from the x-axis of Fig. 3, with their respective coupling capacitances, C_V , specified in the left-hand y-axis. For instance, as can be seen in Fig. 3, for the XOR logic gate, inversions of logic 1 to logic 0 are found at $3/16 V_{DD}$, $5/16 V_{DD}$, $9/16 V_{DD}$, $12/16 V_{DD}$, and $15/16 V_{DD}$. The external voltages applied to achieve XNOR, NOR, AND, NAND and OR gates can be consulted in [18] for $V_{DD} = 5$ V. It is important to mention that at the output of the programmable inverters, conventional CMOS inverters are needed for signal regeneration [14].

4 TLG-ALU circuit design

More details about the design procedure of the individual TLG are presented in [18]. This procedure was applied in the design of a basic ALU to demonstrate the viability of the operation of this approach. The basic cell of the ALU is based on a logic XOR gate, which is used as part of the necessary adder to implement the logic and arithmetic operations performed by TLG-ALU. The inputs to the adder are three 4-bit summands: A, B and the carry input C_{in} . The outputs of the full adder are F (sum) and G (carry out), respectively. The analysed output functions are the well-known expressions of an adder with three digital inputs, which are described as

$$F(\text{sum}) = A \oplus B \oplus C_{in} \quad (5)$$

$$G(\text{carry out}) = AB + (A \oplus B)C_{in} \quad (6)$$

Although only two arithmetic and two logic functions are analysed with this proposal, a variety of operations can be performed. In particular, the operations arbitrarily selected to be performed with this ALU are expressed as

$$\text{Logic: } AB, A \oplus B \quad (7)$$

$$\text{Arithmetic: } A + B, AB - 1 \quad (8)$$

The type of operation can be selected and also controlled with a 4-bit input signal ($S3, S2, S1$, and $S0$) that will be shown later. To evaluate the performance of the TLG-ALU, the response obtained after of the simulation with ORCAD will be compared with an

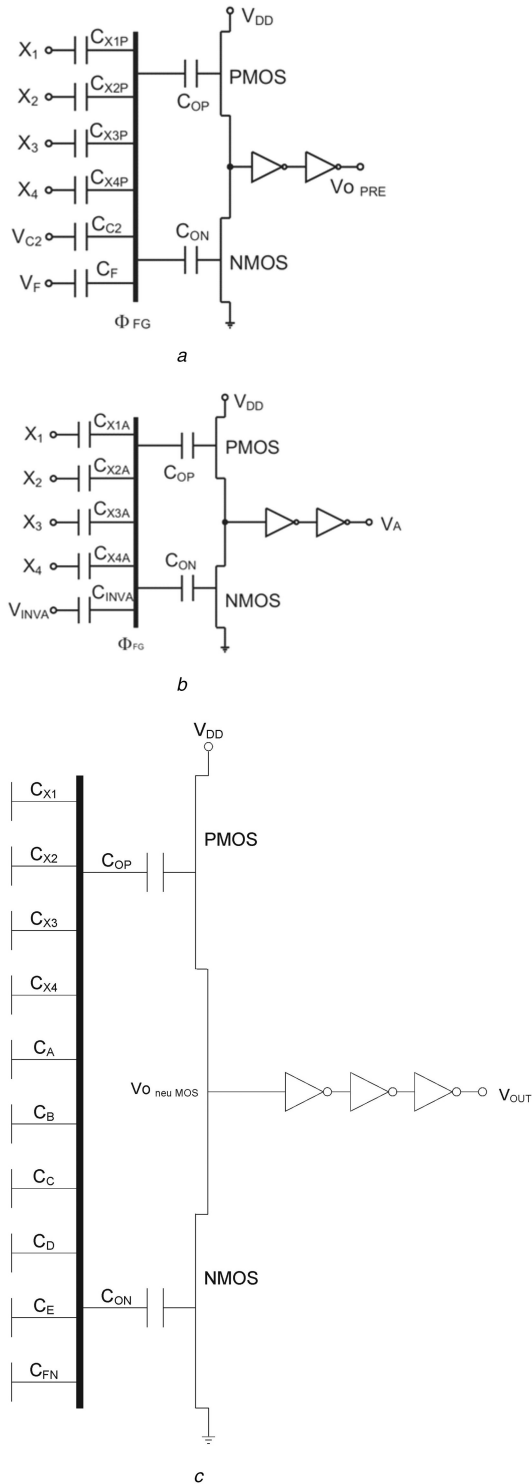


Fig. 5 Schematic diagram of the universal circuit used for logic gates configured with TLG
 (a) Input of the pre-charge stage, (b) Programmable inverter, (c) v-CMOS inverter

ALU synthesised by using: (i) the Spartan 3E evaluation kit from Xilinx and (ii) the ALU chip MC14581B from Motorola.

4.1 XOR circuit block

Each block presented in the basic configuration of Fig. 2 is specifically substituted with the equivalent circuits presented in Fig. 5 for the TLG-ALU simulation. Here, voltage-controlled voltage sources are used to represent the floating gate voltage of the three previous stages on the v-CMOS technology [18].

4.2 Operational blocks f_1 and f_2

In addition to the XOR block of the proposed ALU, the TLG blocks must be added to obtain the desired logic and arithmetic functions expressed in (6) and (7). These blocks are used for the implementation of the function f_1 and the function f_2 , establishing the following considerations:

- Block f_1 is used to implement the logic operation AB , whereas block f_2 is used to implement '0' function so that the operation $(AB) \oplus 0 = AB$ can be performed as a previous partial logical operation before the C_n function can be completed.
- Again, block f_1 is used to implement the logic operation $(A \oplus B)$, whereas block f_2 is used to implement the '0' function as before to perform the logic operation $(A \oplus B) \oplus 0 = (A \oplus B)$.
- For the proposed arithmetic operation $A + B$, block f_1 must enable the variable A , whereas f_2 must enable variable B , so that the operation $A \oplus B = A + B$ can be obtained.
- Finally, for the arithmetic operation $AB - 1$, f_1 must enable the function AB and block f_2 must enable the function '1', respectively, to complete the selected arithmetic operation $AB \oplus 1 = AB - 1$.

Considering two 4-bit input variables (A and B), the blocks for XOR, f_1 , f_2 , and f_{carry} are interconnected as shown in Fig. 6 for a reconfigurable ALU. Each of the selected functions can be enabled using the selection bus S_3 , S_2 , S_1 , and S_0 illustrated in Fig. 6 using the combinations shown in Tables 1 and 2. Here, the outputs X and Y are, in turn, the inputs to both, the XOR and f_{carry} blocks in Fig. 6.

In the proposed circuit, there are two 4-bit variables; then four blocks have to be used in this design, one for each element of the input vector (0, 1, 2, 3). Next, the FPDs for f_1 and f_2 have to be plotted together with the logic output previously defined in Tables 1 and 2, respectively, so that the corresponding input weighted capacitances and transition levels of the programmable inverters used in each block can be graphically deduced to configure the operational blocks f_1 and f_2 used in the design of the TLG-ALU. Figs. 7 and 8 show the FPD graphs according to the outputs X and Y that are expressed in Tables 1 and 2 based on the function to be performed. In this way, values in columns X and Y are specified in the top of each plot, see Figs. 7 and 8, respectively. Table 3 summarises the operation of the ALU unit based on the selection key bits and presents the truth table of the circuit diagram shown in Fig. 6.

4.3 Sum carry block f_{carry}

The element used in the configuration of the adder that handles the carry is represented by the truth table shown in Table 4. Inputs X and Y correspond to the output from blocks f_1 and f_2 , respectively. Fig. 9 shows the corresponding FPD for the f_{carry} function of the adder, this graph plots all possible combinations for a 4-bit vector although the adder will have only three input bits: X , Y and C_{in} . Then, column f_{carry} from Table 4 is limited to the maximum digital count of '111'. Therefore, only the first half of Fig. 9 must be considered in the derivation of the coupling capacitances and the external voltages for programmable inverters.

Reviewing Figs. 3, 7 and 8 it is observed that when the value of ϕ_{FG} is above the threshold line, the output of the v-CMOS is a logic '1'; otherwise, the output is a logic '0'.

4.4 Results

The proposed ALU can handle $24 \times 24 = 256$ different input combinations, and some arbitrarily-selected examples will be presented. However, the tests that cover all options, showed full functionality of arithmetic and logical operations of the TLG-ALU circuit. Then, the logical and arithmetic function outputs are shown only for some input combinations, as indicated in each operation.

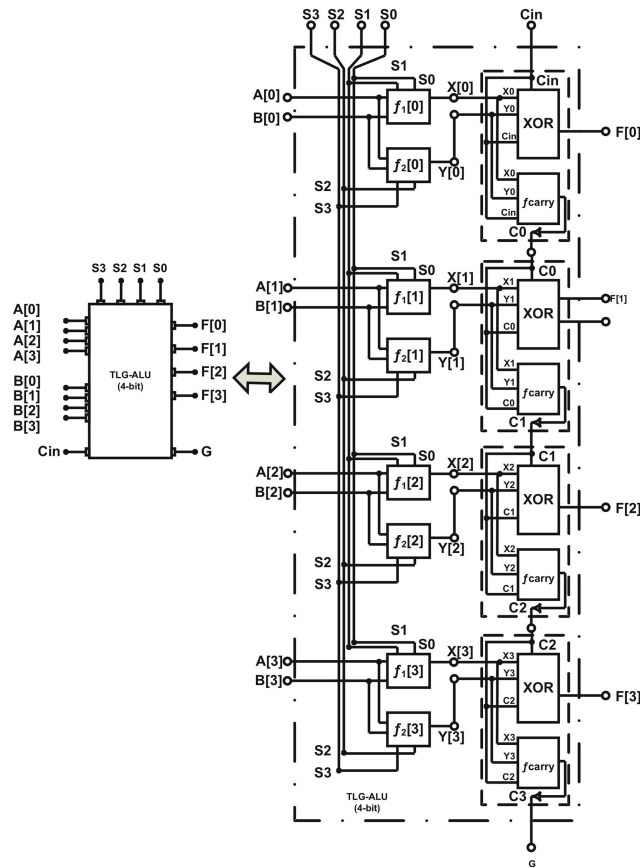


Fig. 6 Proposed ALU using TLG
 (a) Top module, (b) Block diagram presenting main modules

Table 1 Selection of the operation in the block f_i

Selection bits		Input		Output	Function
S1	S0	B	A	X	
0	0	0	0	0	AB
		0	1	0	
		1	0	0	
		1	1	1	
0	1	0	0	0	A
		0	1	1	
		1	0	0	
		1	1	1	
1	0	0	0	0	B
		0	1	0	
		1	0	1	
		1	1	1	
1	1	0	0	1	$\overline{A \oplus B}$
		0	1	0	
		1	0	0	
		1	1	1	

The frequency used for the characterisation was 826 kHz; the tests performed with higher frequencies showed some glitches in the TLG-ALU and this behaviour can occur due to the model used for the ν -CMOS and the large capacitances needed for coupling input signals to the floating gate. Despite the proper operation described with this methodology, there are still some issues that must be investigated and improved.

For instance, the simulation results, although representative, depending on the model used for the ν -CMOS in TLG. The work is still being conducted concerning the floating-gate MOS transistors. Furthermore, although this design with large capacitances is needed, this disadvantage is compensated by the reduction in the

number of devices required to set a function, compared with the number of transistors needed with conventional MOS devices.

It is important to note that the main advantage and the main contribution is that a circuit can be improved for this type of TLG system due to its capability to be reconfigured towards some other logic or arithmetic functions.

4.5 Arithmetic operations

In this section, two arithmetic operations are presented ($A + B$ and $AB - 1$), where three implementations are shown on a chip, FPGA, and ν -CMOS. The presented results correspond to a single signal

Table 2 Selection of the operation in the block f_2

Selection bits		Input		Output	Function
S3	S2	B	A	Y	
0	0	0	0	0	0
		0	1	0	
		1	0	0	
		1	1	0	
0	1	0	0	0	A
		0	1	1	
		1	0	0	
		1	1	1	
1	0	0	0	0	B
		0	1	0	
		1	0	1	
		1	1	1	
1	1	0	0	1	1
		0	1	1	
		1	0	1	
		1	1	1	

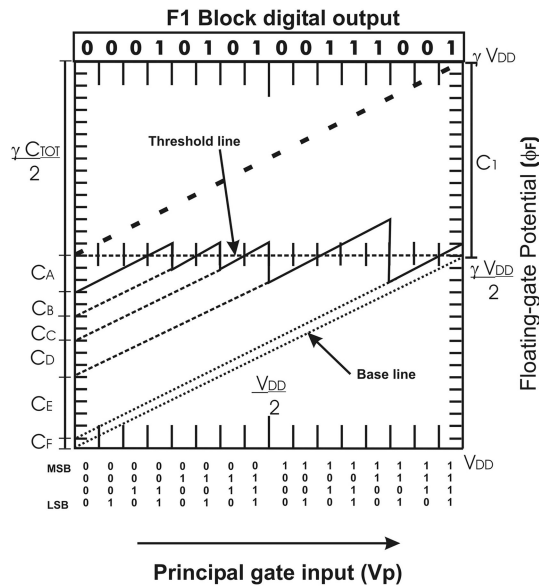


Fig. 7 FPD for block f_1 ; transitions of the programmable inverters for block f_1 must be present at $4/16V_{DD}$, $6/16V_{DD}$, $8/16V_{DD}$ and $13/16V_{DD}$, and values for the coupling capacitances of block f_1 are $C_1 = (16/32)\gamma C_{TOT}$, $C_A = (3/32)\gamma C_{TOT}$, $C_B = (2/32)\gamma C_{TOT}$, $C_C = (2/32)\gamma C_{TOT}$, $C_D = (3/32)\gamma C_{TOT}$, $C_E = (5/32)\gamma C_{TOT}$, and $C_F = (1/32)\gamma C_{TOT}$

window, specifically when $A = [8, 9, 10, 11]$ while $B = [0, \dots, 15]$ for each value of A .

- i. $A + B$: Fig. 10 shows the plot for this operation, first for the measured output to the soft-hardware logic (TLG-ALU), second for the FPGA implementation and, finally, for the Motorola chip. In the output signals presented for each arithmetic operation, $F(0)$ corresponds to the least significant bit, and $F(3)$ corresponds to the most significant bit. For the ALU implementations, these signals show execution with similar results.
- ii. $AB - 1$: This operation is implemented on the same three technologies. Fig. 11 shows the full test-signal window, where vectors A , B , and F are presented. It can be seen that the results are the same in the three cases, although SHL implementation presents a small number of spikes, which has a very small amplitude and can be easily smoothed by using filters.

4.6 Logic operations

In this section, two logic operations are described: (AB and $A \text{ xnor } B$), where three implementations are shown in the chip, FPGA, and γ -CMOS. As described in the previous section, the same conditions of the test values are analysed.

- i. AB : Fig. 12 shows how the similarity of the output of the three implementations. The dotted line indicates the period of the A test value, where B changes 16 different test values. For example, when $A = 0b1010$ and $B = 0b1100$, then output $F = AB = A \text{ and } B = 0b1000$.
- ii. $A \text{ xnor } B$: Finally, Fig. 13 shows the test vectors for the three implementations. In the same way, as in the previous operation, the dotted line indicates the period of the A test value, where B changes 16 different test values. For example, when $A = 0b1010$ and $B = 0b0000$, then output $F = A \text{ xnor } B = 0b1010 \text{ xnor } 0b0000 = \text{not}(0b1010 \text{ xor } 0b0000) = \text{not}(0b1010) = 0b0101$, which can be compared and visualised in the graphic.

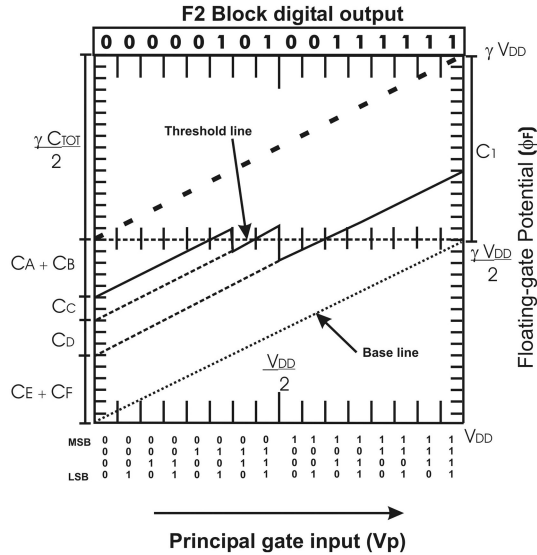


Fig. 8 FPD for block f_2 ; only two transitions can be identified at $6/16V_{DD}$ and $8/16V_{DD}$ and five coupling capacitances with the following magnitudes: $C_F = (1/32)\gamma C_{TOT}$, $C_A + C_B = (5/32)\gamma C_{TOT}$, $C_C = (2/32)\gamma C_{TOT}$, $C_D = (3/32)\gamma C_{TOT}$, and $C_E + C_F = (6/32)\gamma C_{TOT}$

Table 3 ALU functions based on the selection of the control signal

4-bit control signal				Input signal		Function
S3	S2	S1	S0	A	B	
0	0	0	0	A	B	AB
0	0	1	1	A	B	$A \oplus B$
1	0	0	1	A	B	$A + B$
1	1	0	0	A	B	$AB - 1$

Table 4 F_{carry} 's truth table

Y	X	C_{in}	$X + Y$	f_{carry}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4.7 Comparisons

For comparison, a number of transistors are necessary, which depends strictly on the designed circuit (application) and the power dissipation depends on the voltage-power supply computed by (9) of the chip and the current flowing in each device, which is computed as

$$\frac{\beta_p}{2}(V_{DD} - V_{thp} - V_{sp})^2 = \frac{\beta_n}{2}(V_{sp} - V_{thn})^2, \quad (9)$$

$$V_{SP} = \frac{\sqrt{\beta_n/\beta_p} * V_{thn} + (V_{DD} - V_{thp})}{1 + \sqrt{\beta_n/\beta_p}}. \quad (10)$$

The physical implementation of the proposed ALU is shown in Figs. 14 and 15. The first presents the basic layout cell for the main components of the ALU: 4-bit adder, which contains f_{carry} and XOR blocks, see Fig. 14a, and f_1 and f_2 blocks, see Fig. 14b. Additionally, a diverse semiconductor material is used, which is listed in the down of the figure.

Additionally, Fig. 15 presents the layout of the SHL circuit for the 4-bit ALU, where the input/output ports and the cell ν -CMOS are plotted. This is manufactured by MOSIS, which provides different implementation metrics and parameters, such as area, number of transistors, power dissipation, and so on.

Specifically, the number of transistors depends on the discrete design and the layout of the SHL circuit designed and manufactured in MOS technology, see Table 5. At this point, the ν -MOS is a multi-input floating gate transistor that has multiple control inputs (floating gate). This technology applied in systems with large scale integration drastically reduced the number of transistors; otherwise, the number of transistors in CMOS technology only has one input gate, making the CMOS design to have: (i) a greater number of transistors for integrated high-scale ICs, and (ii) a greater number of interconnections. For example, using the SHL technique, a full adder can be made using only 8 ν -MOS transistors while a design using conventional CMOS gates will use 50 transistors [3]. However, a drawback of the SHL implementations is the large capacitance created by the weighted inputs, which generate greater area and affect the speed of the logic. The number of transistors used for the SHL ALU 4-bit chip design is 112 transistors, where 30 transistors are used in the pre-charge stage, six transistors for each programmable inverter, and eight transistors in the neuron stage. Compared with the MC12581B chip that is designed with CMOS technology and has a density of 326 transistors, the proposed ALU has a reduction of 66%.

The manufacturer, called MOSIS Service, produced the chip and generated the report containing the manufacturing results and measurements of the MOSIS test structures on each wafer of the fabrication lot, where the measurements on a selected wafer are similar by using parameters and simulations in the tool SPICE. The important results of this work are: (a) the frequency clock is 37.97 MHz at 5.0 V, (b) the power dissipation per gate of the transistor at the operating frequency is $1.57 \mu W/MHz/gate$, (c) the number of transistors and power consumption, where the commercial chip uses 324 transistors with a power consumption of 200 mW, while the proposed circuit has 112 transistors and consumes 79.2 mW, that is, 66% less power because of the interconnection density, (d) number of pines is 40, (e) technology is SCNA with $\lambda = 0.8$, (f) the layout size is $2181 \times 2181 \mu m$, and (g) the SHL chip design area is $4.757 mm^2$.

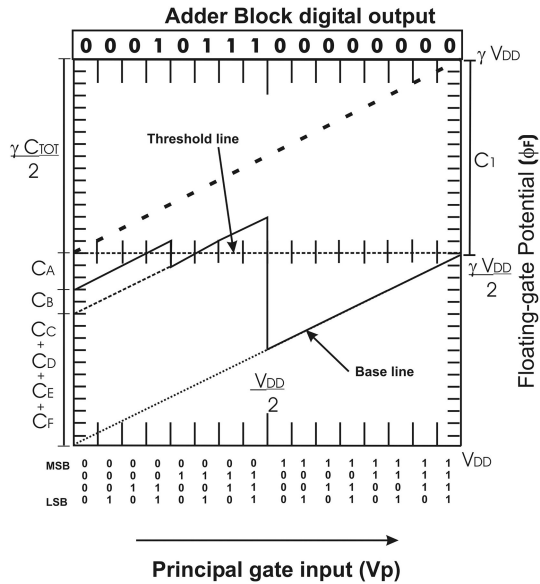


Fig. 9 FPD for the adder block; transitions are located at $0/16V_{DD}$, $4/16V_{DD}$ and $8/16V_{DD}$ and the coupling capacitances should have the following ratios: $C_A = (3/32)\gamma C_{TOT}$, $C_B = (2/32)\gamma C_{TOT}$, and $C_C + C_D + C_E + C_F = (11/32)\gamma C_{TOT}$

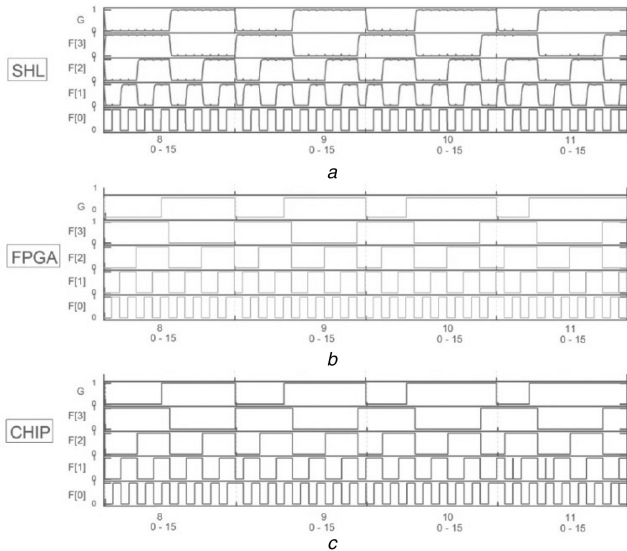


Fig. 10 Output comparison for the three ALU configurations with the arithmetic operation $A + B$

In the proposed ALU, the overhead of the TLG is controlled by the sum of potential in the floating gate, in comparison with the conventionally designed MOSFETs, which strictly depends on the compensation stage.

At first instance, from results in Table 6, it can be observed that the TLG are a feasible option for digital reconfigurable circuits, in spite of the limitations present in the performance of the ν -CMOS such as the frequency operation, power dissipation, and operation control signals. Future work must still be done in order to overcome these limitations.

Recently, researchers are exploring different areas for reconfigurable solutions or floating-gate based solutions. For example, Pengjun *et al.* [20] report a neuron MOS transistor that controls the weighted sum of the multiple-input gate and capacitance coupling effect on the floating gate, which is used for a multiple-valued D/A and A/D converter. Moreover, Kim *et al.* [21] describe an IC design, integration, characterisation, and algorithmic development of an integrated floating gate programming system for a large-scale field-programmable analogue array. In the same way, Hodayoun [22] presents a hybrid design to perform logical vanishing by employing non-volatile

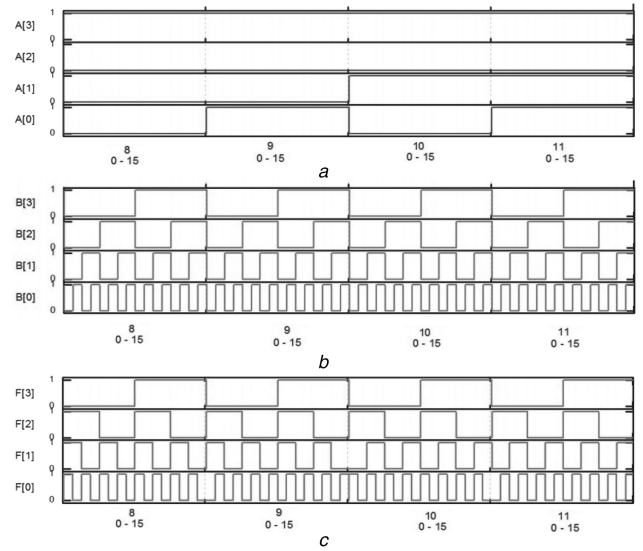


Fig. 11 Execution of operation $AB - 1$ for the three ALU configurations

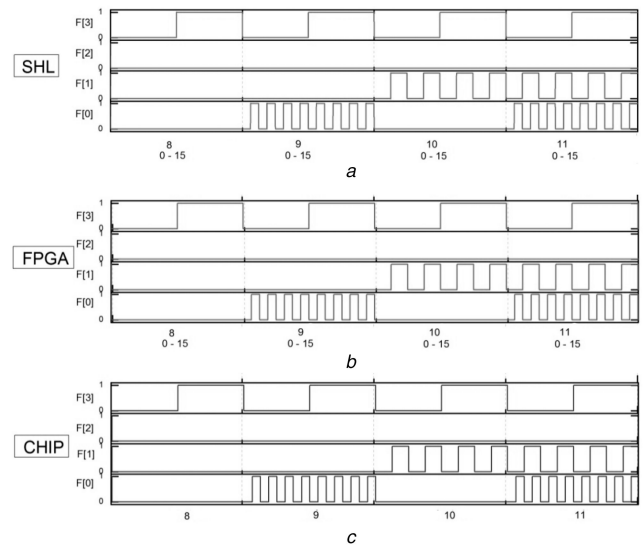


Fig. 12 Output comparison for the three ALU configurations with the AB logic operation

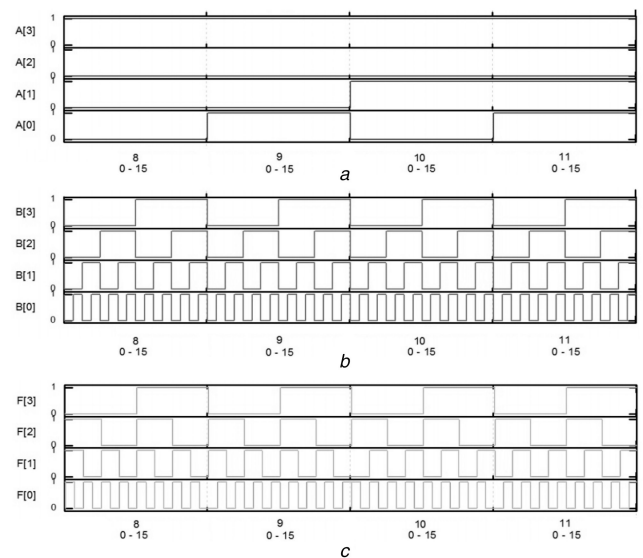


Fig. 13 Execution of the operation $A \text{ xnor } B$ for the three ALU configurations

embedded memory cells, where a look-up-table based on logic components from simple NAND and NOR gates to an array of

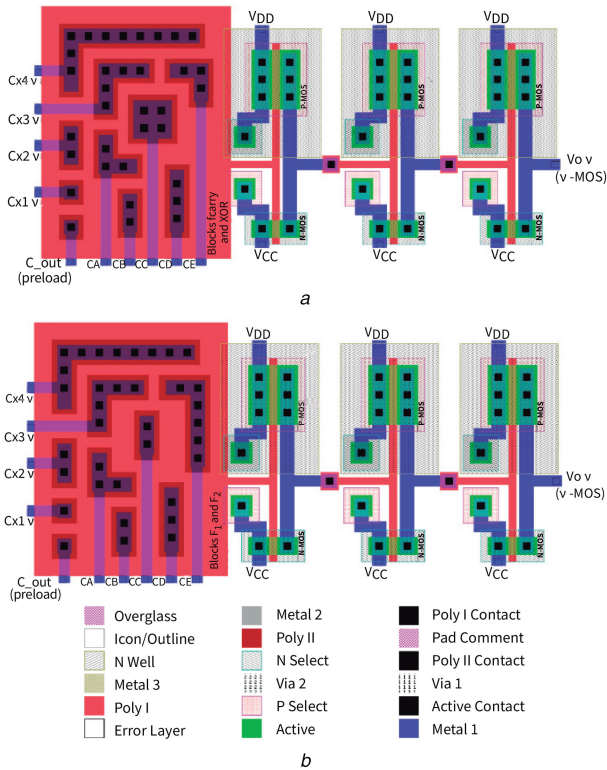


Fig. 14 Layout of the basic cell v-MOS and the control voltage for the (a) 4-bit adder, which contains f_{carry} and XOR blocks, (b) f_1 and f_2 blocks

Type of cell	Number of transistors by cell	Number of cells	Total transistors
pre-load circuit	2	1	2
programmable inverter circuit	2	5	10
v-MOS circuit	2	1	2
4-bit SHL circuit ONLY floating gate transistor	14	1	14
chip 4-bit SHL circuit ONLY floating gate transistor + CMOS	14	8	112

Implementation	Freq., MHz	Number of transistors	Power dissipation, mW
SHL	0.826	112	79.2
FPGA Spartan 3E	94.34	100,000 logic gates close to 80,000 transistors	12
CHIP MC14581B	0.826	324	200

gates providing a complex MAC arithmetic unit, Advanced Encryption Standard engine and, ultimately, the entire processor is developed. In addition, in [23], the authors implement a 4-bit ALU, which is designed and simulated in standard 350 nm CMOS technology and its power consumption is about 120 mW, and the ALU proposed in our research reports 79.2 mW.

Finally, there are other design approaches to provide reconfigurable circuits such as carbon nanotubes [24], silicon nanowires at layout level [25], silicon-germanium heterojunction bipolar transistor technology [26], photonics at silicon level and electrons [27]. They are specifically focused on the level of electronic mobility, charge densities, body effects, and mobility in the transistor conduction channel.

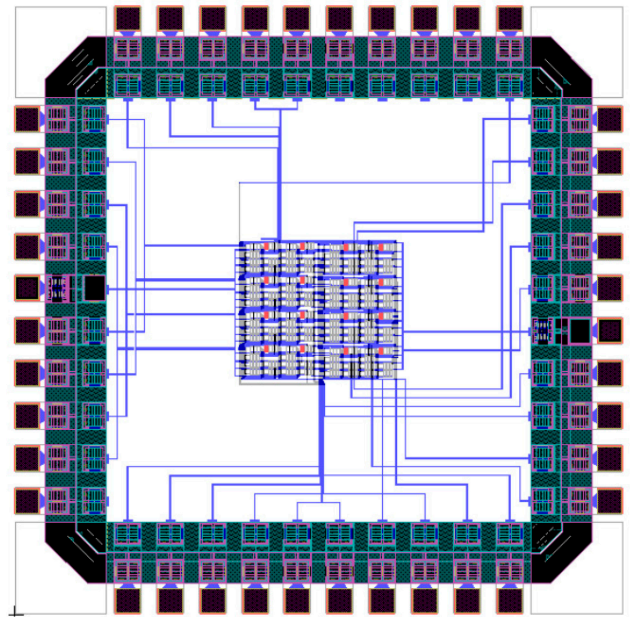


Fig. 15 Layout of the SHL circuit for the 4-bit ALU

5 Conclusion

This research showed that TLG based on v-CMOS circuits are a viable option for reconfigurable circuits since their design offers a reduced number of transistors compared with conventional alternatives. The basic cells can be designed and used for a more complex system design, such as the ALU presented in this work. In addition, it is important to mention that the advantage of this design is that it can be designed considering different polarisation voltages, CMOS technologies and the use of the respective technological parameters. This is possible through the qualitative information obtained from the FPD. On the other hand, using the proposed methodology, we design and compare the proposed ALU with a ALU configured with a commercial chip and with an FPGA evaluation board.

The results are completely consistent among the three designs, showing the feasibility of the methodology based on the floating gates of v-CMOS. Also, a group of two logical operations and two arithmetic operations was shown, producing the same results as those obtained for the commercial chip and an FPGA evaluation board. This methodology can be considered global because the same design can be made for different technologies or circuit polarisation.

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