

Release Optimization of Suspended Membranes in MEMS

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1. Introduction

Releasing part(s) of micro-fabricated devices using etching techniques is one of the fundamental post-processing steps in micro-machining and it is important to have a comprehensive concept on how it can be done, since the final result will significantly influence the electrical and mechanical performance of devices. As micro-electromechanical systems (MEMS) are three dimensional structures, they are obtained by eliminating materials commonly used in this technology, such as crystalline silicon, polycrystalline silicon, silicon dioxide and silicon nitride.

Micro-machining can be undertaken by etching the bulk of the substrate or sacrificial layers deposited at the surface of the wafer. Bulk etching removes great quantities of material and is usually applied to obtain thin membranes for pressure sensors, etching from the back surface of the substrate. On the other hand, surface micro-machining is based in the elimination of sacrificial layers deposited at the surface of a substrate underneath the layers that should be active. The present study will deal only with bulk etching.

Therefore, as several materials are used to obtain finally the typical sensors and actuators in MEMS devices, etching must be selective depending on the material that should be removed. There are available methods for material etching based either on gaseous or liquid etchants. The former employs complex and expensive equipment, but with good yield, and the latter is a low cost process, but care should be taken since in some cases it uses toxic or even corrosive solutions and facilities are needed to exhaust or protect from the vapours produced during etching.

However, both kinds of etching processes are widely used in MEMS and CMOS technology and this fact can be conveniently used to match both technologies, so complete MEMS devices can be integrated in the same substrate, reducing fabrication costs. In particular, wet etching can be either isotropic if material is removed uniformly in all crystallographic directions or anisotropic if etching is selective to a given crystallographic plane.

With regard to anisotropic etching, two solutions are commonly used like potassium hydroxide (KOH) and trimethyl ammonium hydroxide (TMAH). Both solutions are regularly used in MEMS technology to obtain structures, such as thin membranes and

cantilevers. The present study gives emphasis to the properties of TMAH and how it acts in silicon upon different geometries designed to obtain a thin membrane used in semiconductor gas sensors (SGS) with the objective to reduce etching time so damage to materials different to silicon can be minimized.

As the convenience to keep compatibility between MEMS technology and CMOS integrated circuits technologies has been demonstrated, it is important to apply etching techniques without damaging the layers used as masks. Within the criteria that should be considered is the etching time since optimum processes must be applied so well defined tridimensional structures can be perfectly obtained at any time.

Based on crystallographic concepts and the way TMAH acts during silicon etching, the main purpose of the present study is to demonstrate the effect in etching time using a given geometry for the suspended membranes. It will be shown that improvement can be achieved using a specific geometry outline, compared with other options. Knowledge of the influence of size and orientation of the geometric elements on the anisotropic etching made on wafers with (100) orientation can help to optimize the designing process, as will be shown. Simulations were made with the help of specialized software and experimentally confirmed.

2. MEMS etching process compatible with CMOS technology

Micro-electromechanical systems (MEMS) are devices designed for specific sensing of actuating functions based on tridimensional structures and mechanisms that can be fabricated with a set of known micro-machining steps being compatible with mature CMOS technologies used in micro-electronics for the fabrication of silicon integrated circuits.

Actually, those systems find wide application in diverse disciplines since their main functions as sensors and actuators at micro- and nano scale allow, for instance, size reduction of measurement instrumentation. Besides, the development followed by these devices has significantly influenced the creation of elements, such as optics for telecommunications, RF devices, analytic instrumentation, biomedics, optic systems for image processing, micro-fluidics, mechanical supports, etc.

It is clear that these tridimensional micro-structures (sensors and actuators) need an electronic circuit to operate properly as they interact with the environment to complete a desired function based on input or output signals. Configurations like analogue-to-digital converters, digital memories, artificial neural networks, temperature controllers, etc., are some of the circuits helping in tasks like signal reading or conditioning in domains like digital, analogue or mixed electronic circuits. Therefore, MEMS are considered systems that consist on several blocks with specific features integrated around to deliver or perform a particular function.

One way this integration can be done is to interface the sensors or actuators with separated micro-modules. Each of them (tridimensional structures and modules) are fabricated in a separate chip then connected and packaged together. The advantage of this alternative is the independence in the fabrication technology of each block, applying particular convenient steps to meet specific purposes, i.e. etching on one side and micro-electronics on the other.

Then, both are packaged and interconnected to configure the complete system. However, a great disadvantage that this alternative presents is that stray capacitance is added affecting the performance of the device. Also, packaging of the modules can be highly complex adding the chance of device failure and yield reduction as a consequence (Korvink & Paul, 2006).

Therefore, a good choice is to monolithically integrate the system in the same substrate, where sensors or actuators are placed next to the electronics in the same technological process where MEMS and circuitry are fabricated, eliminating extra interconnections, reducing the area of the system and increasing the yield. A clever design can give high compatibility among the different blocks used in the system and the packaging process.

Nevertheless, this apparent simplicity is true only for MEMS fabricated using compatible CMOS technologies. However, care should be taken to eliminate or reduce damage to layers and materials used as protection masks. So, the main goal is to process the chip without risk or damage to the masking layers when micro-machining the typical three dimensional structures needed as sensors or actuators.

Due to this limitation, it is important to optimize the geometric design of the structures in order to assure the physical integrity of the different layers used in the fabrication of an integrated circuit, as well as to keep the compatibility of MEMS fabrication with CMOS technologies (Baltes, 2005). One of the main advantages of this alternative is the reduction in production costs since a high number of devices can be fabricated in batch run.

It should be remembered that micro-machining is, in general, a set of techniques and tools used to obtain tridimensional elements and structures with high precision and good repeatability by adding or removing layers in a controlled way.

A basic technique in MEMS is volumetric wet etching, when an etching is made to a substrate thick enough with a solution prepared with certain elements that react with it, eliminating part of the substrate. The amount of material etched away depends on the kind and conditions of the solution used, like temperature, concentration, etching time, stirring and the crystallographic orientation of the substrate.

Materials used as protective masks also play an important role in the micro-machining process so the desired structure can be readily obtained. Hence it is important to keep in mind the type of substrate and layers that will be used in the fabrication of the integrated circuit that will contain MEMS, since this will indicate which solution must be used for micro-machining (Hsu, 2002).

Usually, volumetric wet etching is used with silicon substrates for the fabrication of structures like micro-cavities, thin membranes, through holes, beams and cantilevers, taking advantage of the structural layers included in CMOS integrated circuits' technology.

This kind of wet etching can be classified as isotropic and anisotropic. The first has a uniform etch rate to the substrate in all crystallographic directions of silicon, and the second is selective on the crystallographic direction, that is, the etch rate is higher on those directions whose atom density is not too high.

3. Suspended membranes and applications

The case presented here deals with membranes fabricated with anisotropic wet etching of a silicon substrate. These kinds of structures are also thin layers that can operate as sensors and mechanical support for the circuitry. Within the most common applications for these membranes, there are piezoresistive pressure sensors, micro-hotplates and pyroelectric sensors, among others (Barrettino et al., 2004a, 2004b; Capone et al., 2003; Chen et al., 2008; Gaitan et al., 1993; Tabata, 1995)

In general, these structures are fabricated etching the substrate from the back side of a silicon wafer, where no electronic devices are present. This method allows perfect protection

of devices placed at the front of the wafer when the compatibility of the layers used is limited, using a mechanical mask or a protective film.

Likewise, this kind of process simplifies the design of the structures that are to be etched, since this step does not affect the geometric configuration of the circuitry at the other side of the wafer. However, a main disadvantage is the large area used for the definition of the membrane due to the characteristics of the anisotropic etching (Madou, 2001). Typical shapes obtained with anisotropic etching using trimethyl ammonium hydroxide and water (TMAHW) are shown in Fig. 1.

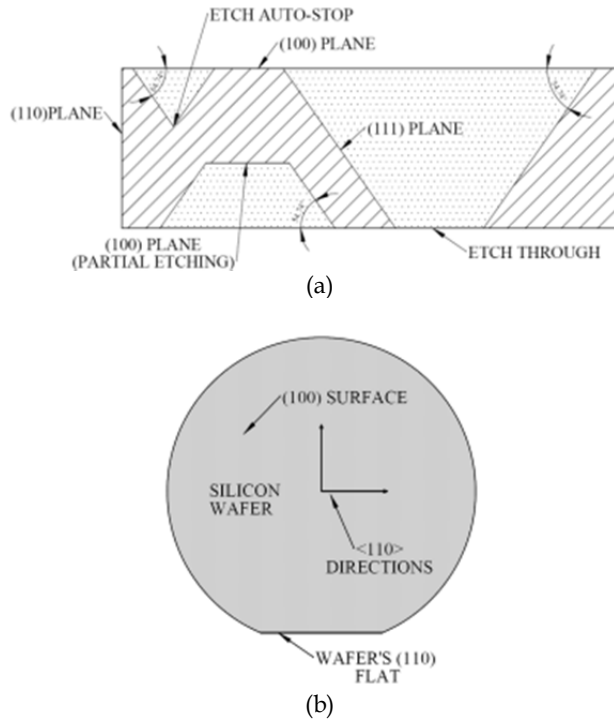


Fig. 1. Anisotropic etching of a silicon substrate.

Nevertheless, it is obvious that this technique takes a long time to complete the etching because the wafer is usually too thick and the etch rate of TMAHW is around 1 micron per minute. Also, this back side etching requires simultaneous alignment at the top and back of the wafer (double alignment) in order to perfectly define the needed structure. So this step introduces an extra restriction to achieve the thin membrane.

On the other hand, this membrane can also be obtained with an etching process made at the front surface of the wafer. This is called front bulk etching, a process also frequently used in MEMS. Although it is made at the front surface of the wafer, it is still considered bulk etching since no surface sacrificial layers are removed to obtain the thin membrane, whereas bulk silicon beneath the defined membrane area is etched away. As with the back etching, with the front silicon etching process it is also needed to protect those areas that will not be part of the tridimensional structure.

Since the front part of the wafer is where the CMOS electronic devices are placed, metal layers are present as well, and they should be protected against the etching solution. Therefore, here the solution should be modified with additives so this solution can selectively etch only silicon when an etching CMOS post-process is applied to an integrated circuit chip. Some commercial products are available and used for protection purposes as an alternative. With this front etching, the design topology of the desired structures must be modified to expose only the silicon areas that must be etched away, taking care not to unprotect the remaining surface where the electronic devices are present.

Comparing back and front etching, it is obvious that the latter takes less time to complete the membrane since etching is carried out just a few microns down from the surface of the silicon wafer, not through almost all the bulk of the substrate. Besides, the area needed to obtain the complete structure is less than that needed with back etching, despite the characteristics of the anisotropic etching, since a shallower inverted truncated pyramid is obtained.

The membrane obtained with front etching is a suspended structure mechanically supported by two or more thin arms, with a central area as the active part of the membrane. Here it can contain circuitry or some other kind of devices having specific functions for the system's operation. The definition of the membrane's area is given with "etching windows" through which selected silicon areas are left exposed.

This can be achieved using appropriate layer layout to generate a CIF of GDS file used for the CMOS integrated circuit fabrication at the silicon foundry. Hence, the solution will only etch the exposed bulk silicon and the rest of the surface will remain protected with an overglass layer commonly used to isolate the integrated circuit from environment contamination before packaging. So compatibility is maintained to a high degree between the steps needed for MEMS fabrication and CMOS technology (Tabata, 1998; Tea et al., 1997).

As mentioned before, the etching solution used in this work for the delineation of the membranes was TMAHW, which is typical for anisotropic etching. This solution has different etch rates depending on the crystallographic orientation of the silicon substrate. Generally, rates for planes {100}, {110} and {111} are the most used in this kind of task, although other orientations could also be useful for etching purposes as high etch rates can be achieved.

Etch rates using TMAHW depend also on the temperature and concentration of the reactive. In particular, the study presented here was made with a concentration of 10% of TMAH and 90% of deionized water at 80°C, from which an etch rate of approximately 0.72 $\mu\text{m}/\text{min}$ was obtained for a {100} plane.

TMAH was used since it is highly selective for silicon etching allowing the use of SiO_2 as the protective mask against etching. This is an important issue because SiO_2 is one of the layers used through the fabrication of CMOS integrated circuits and there is no need to add extra layers that are not used in this technology.

Taking advantage of the photolithographic steps with an appropriate knowledge of the fabrication steps, the etching areas can be easily defined. Therefore, compatibility between etching and the layers used in the fabrication of CMOS integrated circuits is maintained.

It should be mentioned that the designed geometry in the mask will determine the final shape of the anisotropic etching. One of the most important features in this process is the way the etching proceeds in time with regard to the corners of the geometry i.e. concave or convex. It was found that with TMAH, when concave corners are aligned with a {110} plane, etching will stop at the moment when faces with {111} planes coincide, i.e. in the vertex formed by a {100} plane.

On the other hand, convex corners will generate $\{111\}$ planes as well, but in the vertex of the adjacent planes, etching continues below the corner, etching away other planes and releasing the structure so defined. Fig. 2 shows a mask for a cantilever where the corresponding corners are indicated (Kovacs et al., 1998).

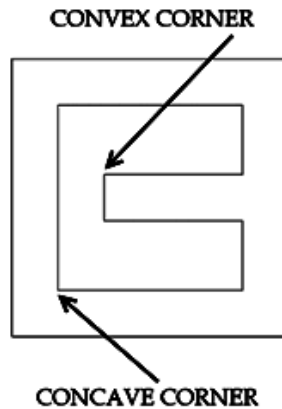


Fig. 2. Geometry of a cantilever illustrating convex and concave corners.

Furthermore, suppose there is a window with an irregular opening, such as the one shown in Fig. 3. The characteristic etching self-alignment with respect to the crystallographic planes due to the anisotropy will be evident.

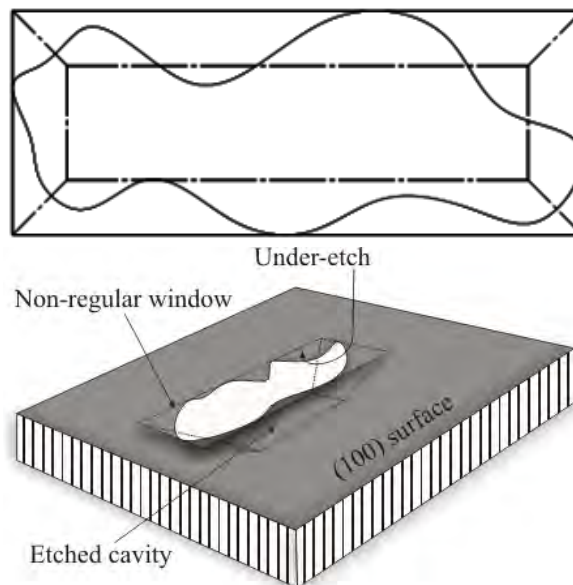


Fig. 3. Etching resulting from an irregular open window.

Dealing with anisotropic etching, there is a feature that is important to consider. When the motifs are aligned with {100} planes, {100} walls will be obtained that are etched as the wafer surface.

4. Geometry and optimization of the suspended membranes

A micro-hotplate was designed to be used in a monolithic CMOS gas sensor which was later fabricated by MOSIS. Then, an anisotropic etching process was performed on the chip using TMAHW, following several formulations that increase the selectivity of the TMAH to avoid damage to the exposed aluminium on the chip caused by the etching solution (Fujitsuka et al., 2004; Sullivan et al, 2000; Yan et al, 2001).

The next figures show the fabricated chip after a TMAHW etching process.

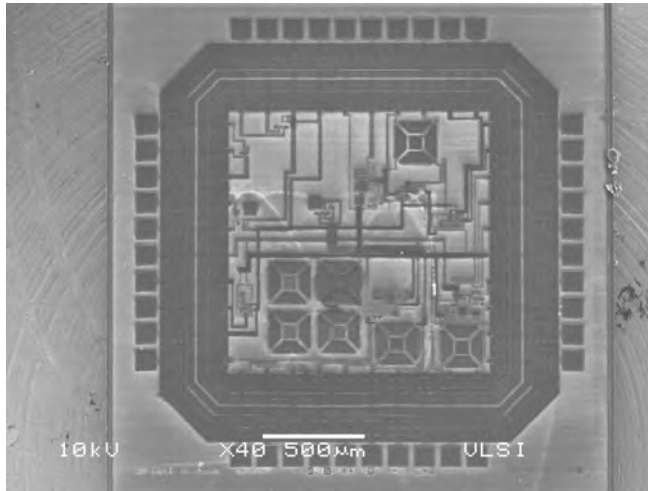


Fig. 4. Fabricated chip after etching.

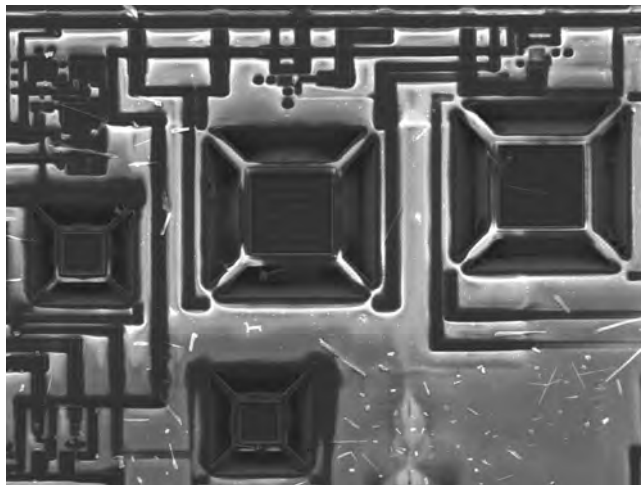


Fig. 5. Partially etched micro-hotplates.

It was found that the aluminium was sometimes still getting damaged by the solution in an unpredictable way and with a limited repeatability. The damage increased as the etching time was increased, so if the etching time can be reduced by a significant amount, the same applies to the damage of exposed aluminium.

Figure 6 shows photographs from before (left) and after etching, where the exposed aluminium is indicated. The damage can be seen.

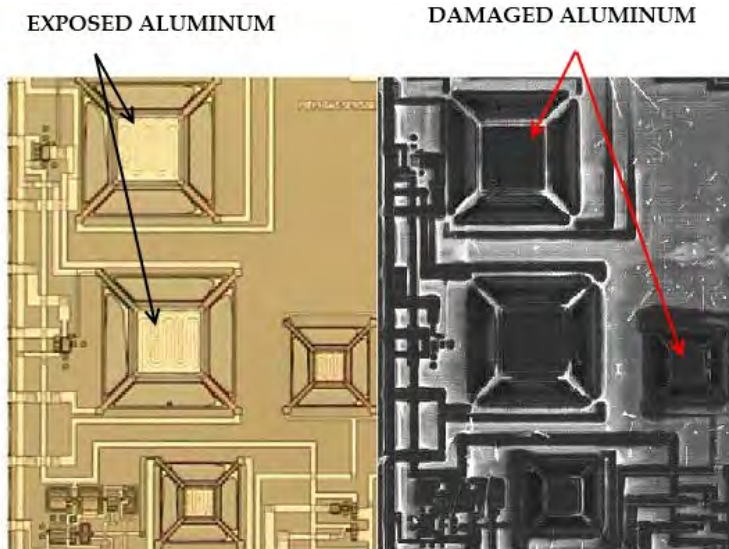


Fig. 6. Comparison between before (left) and after etching.

This motivation is the main objective of this study, which comprises etching and mechanics simulations and the etching of the resulting designs. It should be noted that the designs presented are of micro-hotplates with general applications, as mentioned before.

The most common geometry used for micro-hotplates and suspended membranes are shown in Fig. 7. It can be seen in this figure that the central part of the structure is aligned to $\{110\}$ planes of the substrate, while the supporting arms have an angle of 45° and 135° with respect to the horizontal reference, therefore aligned to $\langle 100 \rangle$ directions (Pierret, 1989). This slope allows other planes to be exposed to the etching solution, hence accelerating the etching process helping to the supporting arms' release. However, this process decelerates when the central part of the membrane is reached, as $\{111\}$ planes are now exposed at this moment. As already indicated, these planes have the lowest etch rate and in this location, the etching proceeds as with convex corners.

From this moment on, etching takes a longer time until the structure is released. If these effects of the etching solution over the main planes exposed by this geometry are analyzed, alternatives can be found for geometries such that planes with a high etching rate can be readily exposed. For instance, if exposing $\{111\}$ planes can be avoided or reduced; the consequence will be immediately reflected in a reduction in the etching time.

With this motivation in mind, a study of alternatives for the geometry of the micro-hotplate follows, directed to the reduction of the etching time and the corresponding effects. These

two objectives were simulated previous to the experimental process with specialized software for anisotropic etching.

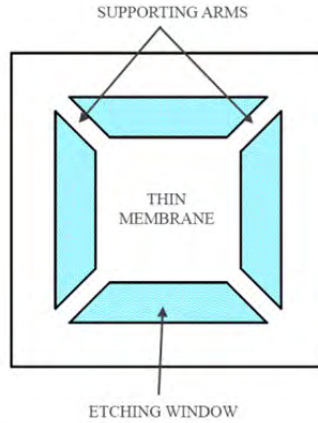


Fig. 7. Common suspended membrane geometry.

4.1 Etching simulations

Features considered in this study for geometry optimization are: a) width of the membrane supporting arms; b) dimensions of the thin membrane; c) orientation of the thin membrane with respect to crystalline planes. Simulations with these considerations were first made with the AnisE software from Intellisuite. The base geometry (A) for the suspended membrane is shown in Fig. 8, having simple dimension ratios among the different elements of the membrane, such as supporting arms, etching windows and membrane area. During simulations, the bulk material considered was silicon and the masking material was exclusively silicon dioxide.

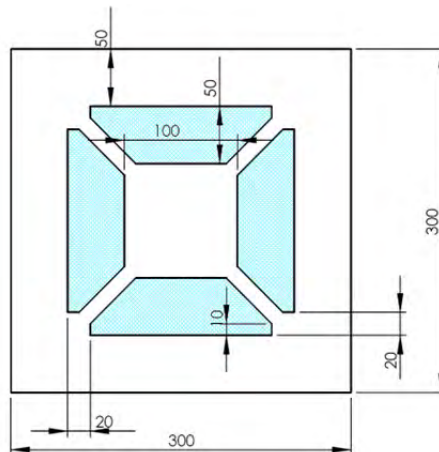


Fig. 8. Dimensions of the base membrane in μm . Geometry A.

First, if the width of supporting arms is increased, it was found that an overlap of the resulting etched areas must exist underneath the arms, proceeding from the exposed silicon windows. This allows for the membrane to be released, otherwise, only four rectangular and separated cavities will be obtained. The required etch overlap is shown in Fig. 9. Due to under etching – always present during the process – this overlap can be a minimum, enough for the supporting arms to be released.

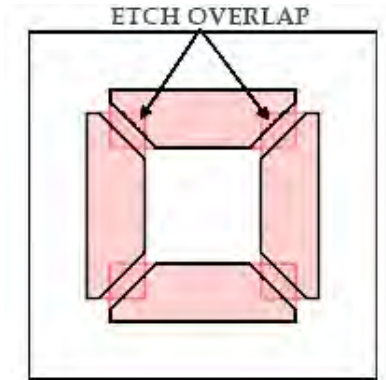


Fig. 9. Geometry A. Etching areas (solid lines) and etching overlaps (shaded).

A 102 min etching time for a complete membrane release was obtained after simulating with the geometry shown in Fig. 8 (Geometry A), with an etch pit depth of about $80\mu\text{m}$. It should be noted from this figure that the etch overlaps extend only across the supporting arms, such that when they are released the substrate under the thin membrane presents $\{111\}$ plane faces to the etching solution, with the same dimensions as the membrane.

Therefore, after release of the supporting arms, the etch rate slows down taking a long time for releasing the thin membrane from the substrate. Then it can be concluded that planes generated at the corners below the supporting arms mainly contribute to the expected etching.

Considering this fact, another geometry (Geometry B) was tested including important overlaps, but that can also avoid features oriented parallel or perpendicular to $\langle 110 \rangle$ orientations that can generate $\{111\}$ planes. It is expected a time reduction in the etching process with this modification, shown in Fig. 10.

As can be seen, the original geometry was rotated 45° with respect to the $\{110\}$ plane reference, keeping the same area. The result obtained from the simulation of this new geometry was an 18% time reduction, that is, the membrane was completely released in 82 min.

One particularity of the geometry shown in Fig. 10 is the reduction of exposed $\{111\}$ planes, since with this alternative, edges being parallel or perpendicular to $\{110\}$ planes are avoided. This reduces both the bulk silicon to be etched away and the etching time.

Next, a new geometry (shown in Fig. 11a) was explored and will be identified as Geometry C. The difference with respect to geometries A and B, respectively, is that although the membrane is also rotated 45° , the supporting arms are aligned along the edges of the membrane. After simulation, a 27% etch time reduction compared to the results from Geometry A was obtained, since the thin membrane was released after 75 min.

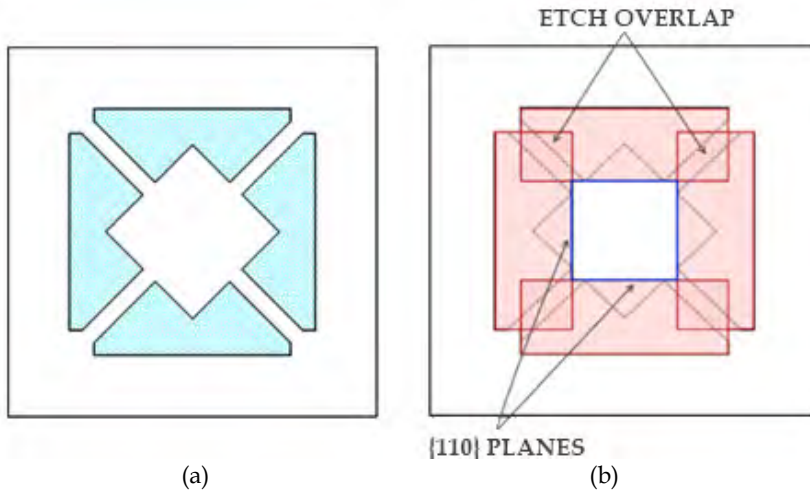


Fig. 10. Geometry B. a) Membrane rotated 45° with respect to $\{110\}$ plane reference; b) Etch overlap.

The reason for the efficiency increase for silicon etching is because with Geometry C there are less $\{111\}$ planes generated at the perimeter of the thin membrane, allowing the underneath silicon to be etched from the beginning of the process, not after the supporting arms are first released.

According to the simulation, the etched pit is approximately $56\mu\text{m}$ deep. The difference between the etched depths obtained with geometries A and B can be attributed to the exposure of larger $\{110\}$ planes, among others, which have a greater etch rate. This is illustrated with the overlaps shown in Fig. 11b.

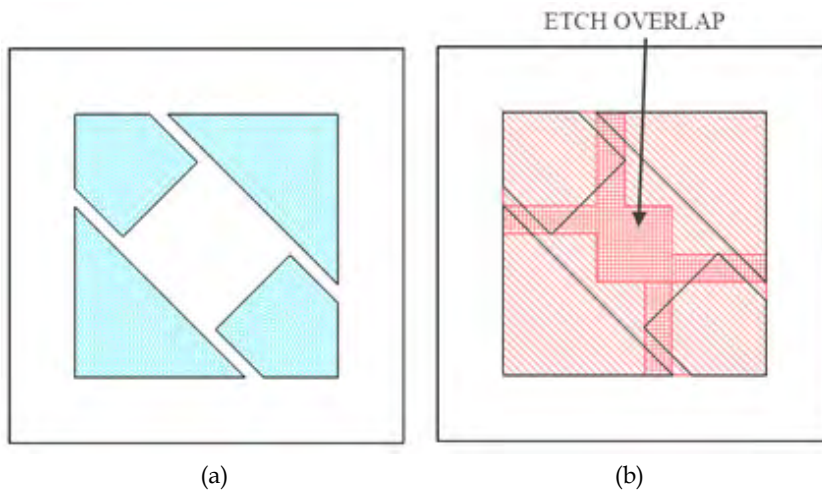


Fig. 11. a) Geometry C; b) Etch overlap.

An alternative for this last geometry is presented in Fig. 12a, where additional supporting arms were added. This will be identified as Geometry D. The purpose for these extra supporting arms is to give mechanical support to the thin membrane so any damage can be prevented if an undesired vibration is suddenly present on the chip. After simulation, this modification showed no improvement in etching time, since the membrane was released also in 75 min with a depth of about $56\mu\text{m}$ for the etched pit. So, compared with Geometry C, it can be considered that the only advantage is the improvement in mechanical support. From Fig. 12b, the difference between the etch overlap areas of Geometry C and Geometry D can be clearly seen.

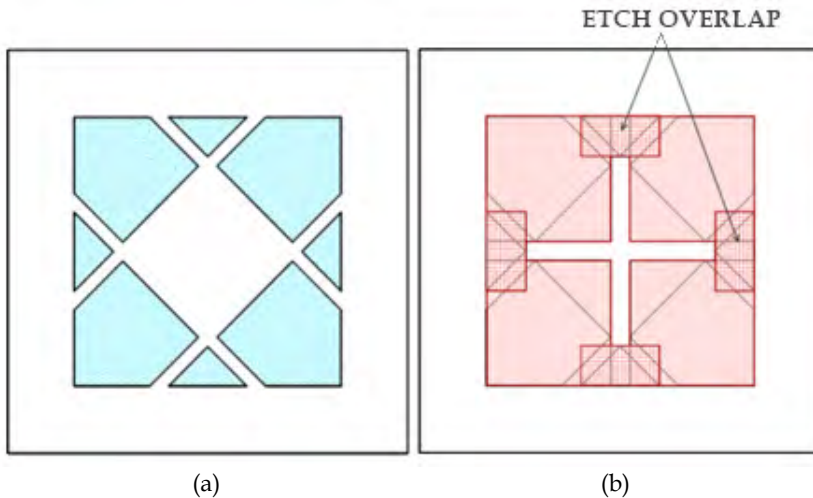


Fig. 12. a) Geometry D; b) Etching areas and etching overlaps.

Although there are no overlaps at the centre, a little substrate area is left (indicated as a thin cross outside the overlaps) that can be rapidly etched away due to its small cross section and the multiple planes present at the vertices of the membrane and the supporting arms.

4.2 Mechanical simulations

Based in a finite element analysis made with COMSOL, the behaviour of the suspended membranes was simulated with each of the geometries described before. Also, in this study it is important to know the weight that the membrane must support. As with restrictions indicated during the mechanical simulation, the extremes of the supporting arms and outer sides of the membrane were set as fixed; the remaining structure should have free movement. The main purpose of the present study was to determine the deformation and stress that exist in the alternative geometries, for comparison purposes.

Geometry A has been widely used and reported in literature and as so, it will be used as the reference geometry to be compared with other geometries. Variables, such as deformation and Von Mises stress, were obtained after simulation in order to evaluate all the membranes, so it can be determined if the proposed modifications introduce some mechanical failure. During simulation, a force equal to the corresponding weight of the

membrane was applied considering also the material from which each membrane is made (SiO_2) and its thickness ($\sim 390\text{nm}$).

For the case of Geometry A, the maximum deformation obtained was $6.357 \times 10^{-15} \mu\text{m}$, with a maximum Von Mises stress of $1.229 \times 10^{-3} \text{MPa}$, that is significantly below the elastic limit for SiO_2 (55 MPa). These results are illustrated in Fig. 13.

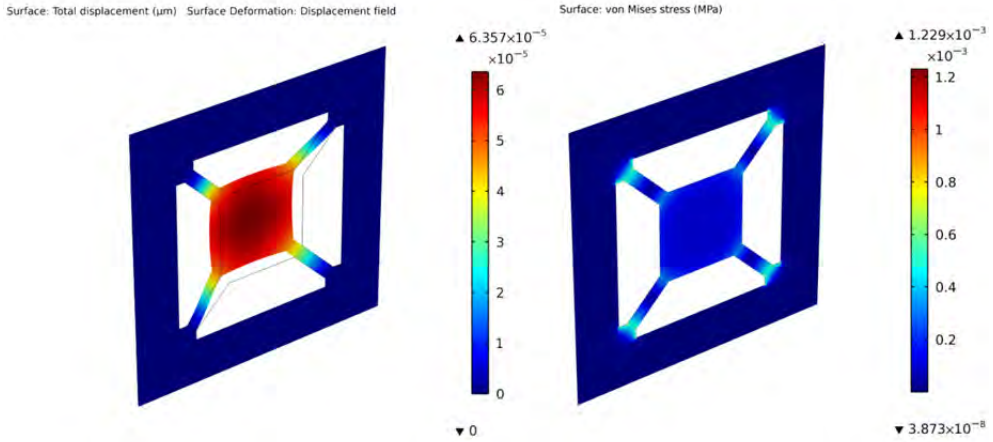


Fig. 13. FEM simulation for Geometry A.

On the other side, the maximum deformation and maximum Von Mises stress obtained in the case for Geometry B were $7.38 \times 10^{-7} \mu\text{m}$ and $1.523 \times 10^{-5} \text{MPa}$, respectively. This strain is also below the elastic limit for SiO_2 . Results are shown in Fig. 14.

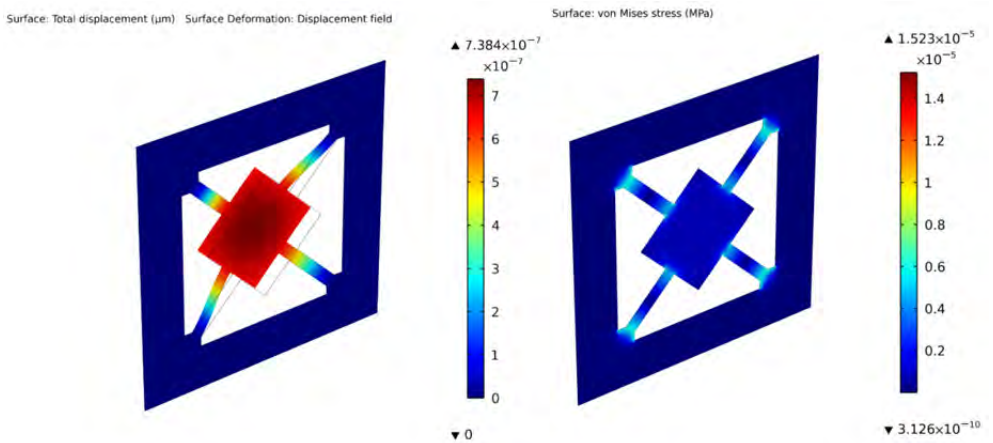


Fig. 14. Deformation and stress for Geometry B.

Next, Geometry C showed a deformation of $2.952 \times 10^{-5} \mu\text{m}$ with a maximum Von Mises stress of $161 \times 10^{-3} \text{MPa}$, showing also that it is a good design from the mechanical point of view. These results are shown in Fig. 15.

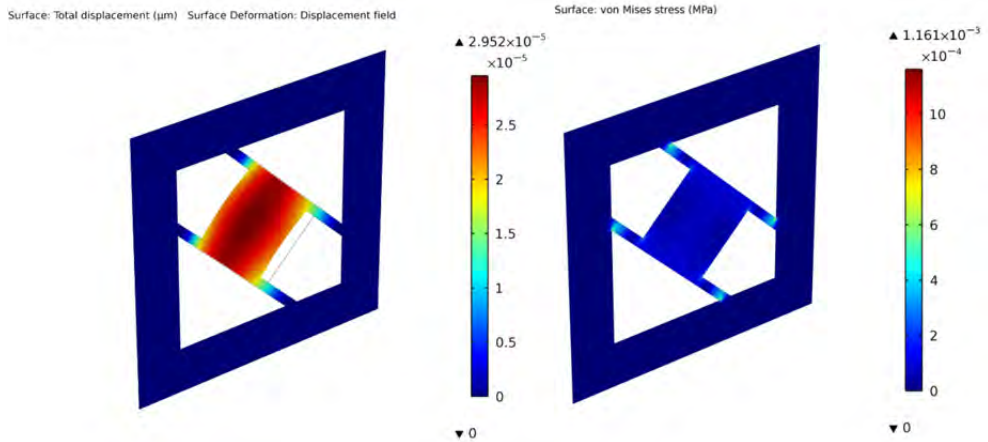


Fig. 15. Simulation results for Geometry C.

Now, Geometry D, having two extra supporting arms, shows a maximum deformation of $2.403 \times 10^{-4} \mu\text{m}$ with a maximum Von Mises stress of $0.01 \times 10^{-3} \text{MPa}$ located next to the arms' anchors. This is illustrated in Fig. 16.

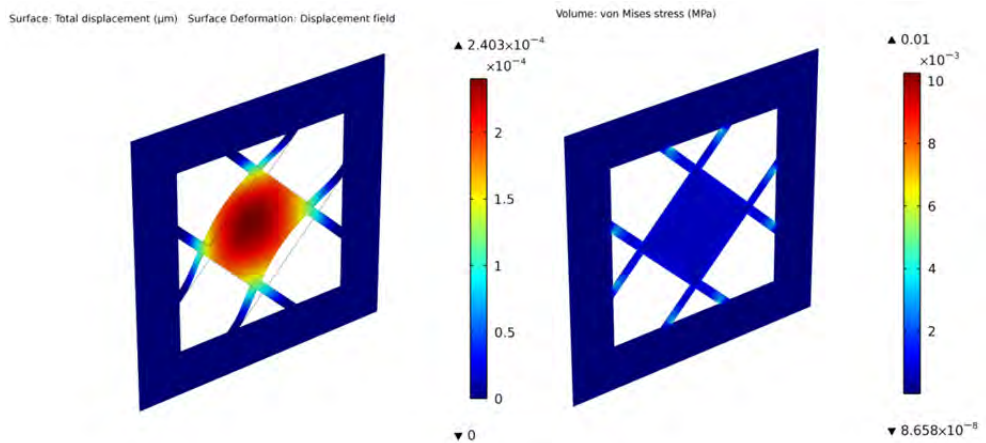


Fig. 16. Mechanical study results of Geometry D.

As is demonstrated, Geometry D shows the highest deformation compared with Geometries A, B and C, but on the other hand, it resulted in the lowest Von Mises strain.

From these results it can be concluded that this geometry is better for the purposes of the present study and also, as will be demonstrated later, with this geometry the supporting arms are released in a considerably shorter etching time.

4.3 Experimental results

Silicon substrates were prepared with a thick silicon dioxide layer (~390nm). Test geometries as those proposed above (A, C and D) were then defined with photolithography. Following, an etching with a 100 ml solution with 10% TMAHW at 80°C added with 1.36 gr of ammonium peroxodisulfate (APS), was done over 25, 50, 75 and 102 min. APS enhanced the sample finishing. This is a common formulation for etching solutions based on TMAHW.

After these times, the samples were checked with a microscope to verify the correct etching. Fig. 17 shows the advance of the etching process for Geometry A where the characteristic figure predicted during simulation is present at the centre of the membrane caused by the anisotropic attack (far left).

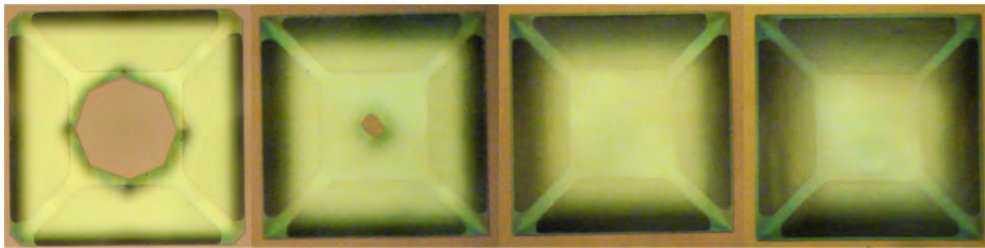


Fig. 17. Geometry A etching photographs.

For Geometry C, Fig. 18 shows the progress of the etching for 25, 50 and 75 min, where the distinctive planes are formed.

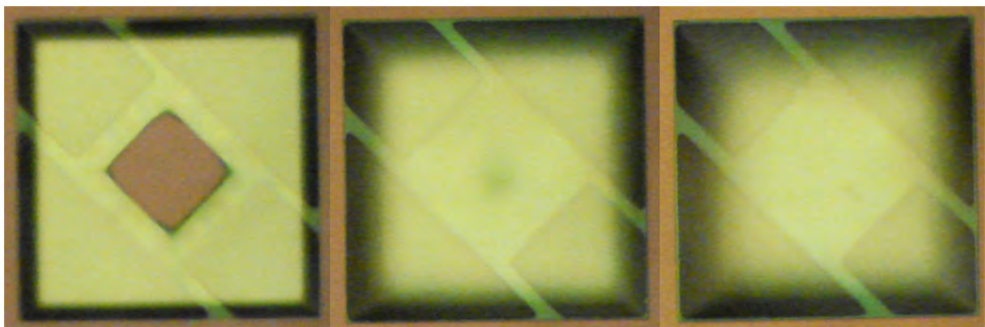


Fig. 18. Microphotographs of Geometry C.

In the same way, Geometry D was processed in TMAH and photographs were taken at the prescribed times. Fig. 19. shows how rapidly the flat bottom formed.

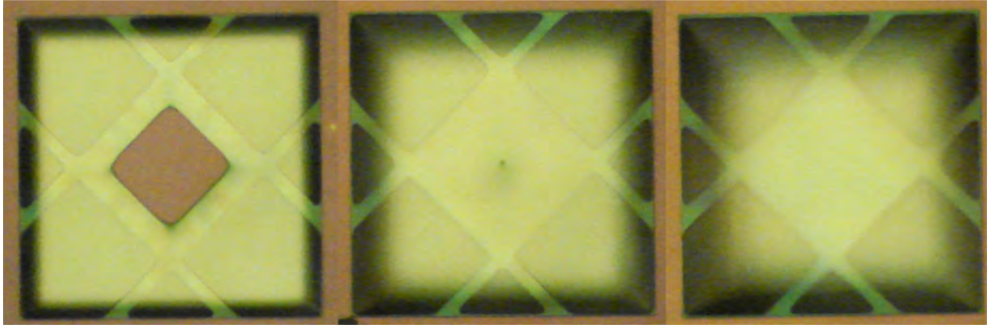
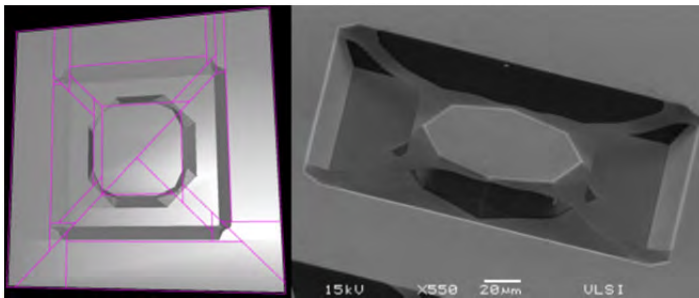


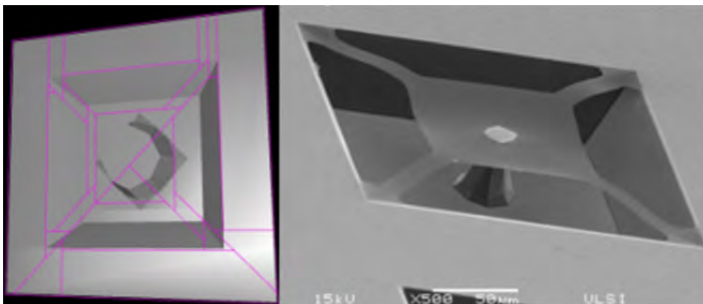
Fig. 19. Geometry D during etching at different times.

Next, results from the experimental etching processes applied are shown and discussed, supported with simulation (left) and SEM images (right).

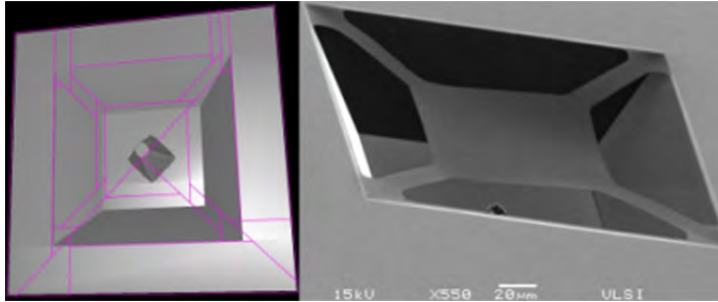
Geometry A.



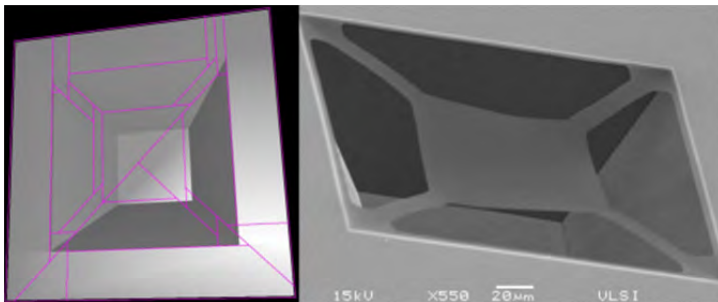
25 minutes: Here it can be seen that after this time, the supporting arms are completely released, but the central bulk of the membrane is just starting to be etched at the corners.



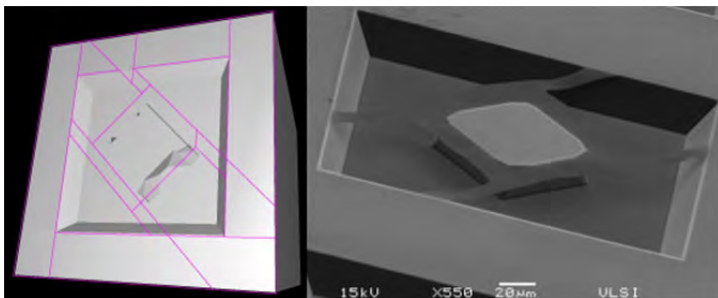
50 minutes: A while later, $\{111\}$ planes generated due to parallel or perpendicular lines to $\{110\}$ planes are completely reduced, but there is still contact between the remaining silicon with the membrane.



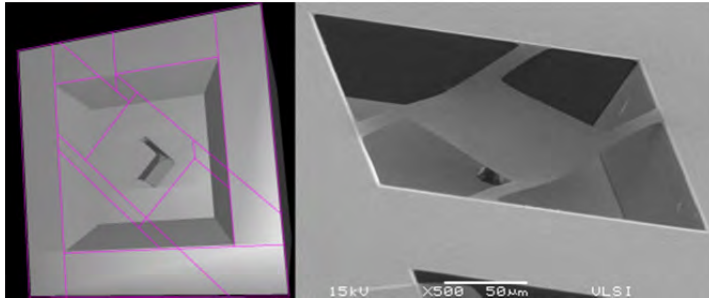
75 minutes: After this time of etching, a square based pyramid shape is formed at the centre of the membrane, having planes from which the etching can continue thoroughly. At this time, there is a little pyramid still left.



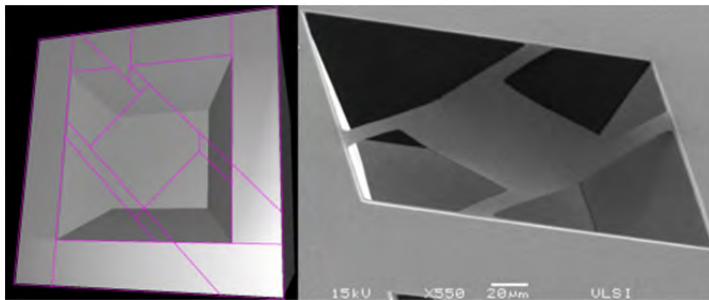
102 minutes: Finally after this time the membrane has been completely released with a bottom cavity surface showing a smooth (100) plane.
Geometry C.



25 minutes: With this geometry, initially the supporting arms are first released exposing {110} planes, that have, as commented before, a high etching rate.

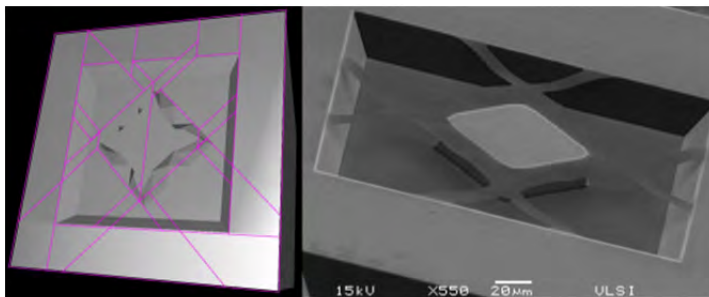


50 minutes: Here it can be seen that a column with $\{110\}$ facets is formed at the centre of the membrane, so etching can continue easily.

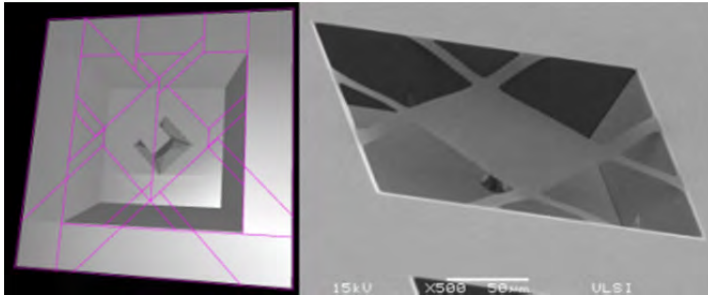


75 minutes: Finally, the membrane was completely released and the cavity has a smooth surface.

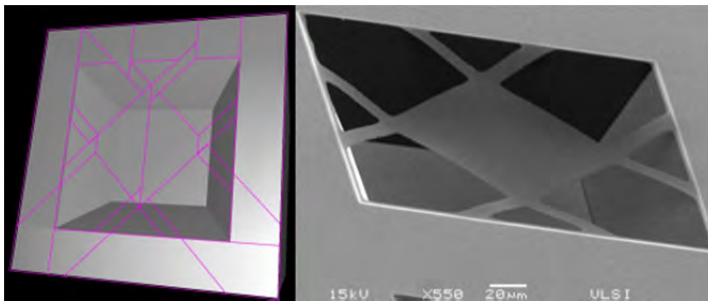
Geometry D.



25 minutes: After this initial etching time, the supporting arms were completely released, but a complex structure is still present having convex corners that can slow down the etching process.



50 minutes: After 25 extra minutes, the substrate of this geometry looks like that obtained after the same time with Geometry C, having also {110} planes with a high etching rate.



75 minutes: Finally, the etching process completely released the membrane also with a smooth cavity bottom.

Comparing the simulation figures and the SEM images from the experimental samples above, it is clear that they are nearly the same, both having a smooth bottom of the cavity, nevertheless, there is a difference in time prediction for the membrane release between theory and experiment.

It may seem clear that the time difference can be attributed to features not considered in AnisE [9] regarding the etching apparatus set, as temperature variations, pH level of the

SUSPENDED MEMBRANE ETCHING			
Structure	Etching time (minutes)		
	Simulated	Experimental	Difference
Geometry A	102	~90	-11%, smooth cavity bottom
Geometry C	75	~72	-0.4%, smooth cavity bottom
Geometry D	75	~72	-0.4%, smooth cavity bottom

Table 1. Suspended membrane etching comparison.

solution and saturation of the solution during the etching process. Despite this difference, the experimental anisotropic etching follows the same behaviour predicted by simulations. Table 1 summarizes these results.

5. Proposed layout for a micro-hotplate

From these results, a new layout for a micro-hotplate has been designed using Geometry D as described above. The micro-hotplate contains a micro-heater made with polysilicon, which will heat the structure when a voltage is applied to the heater terminals. There is a temperature sensor also made with polysilicon which will be connected to a control circuit to maintain the temperature of the micro-hotplate to a given value. Fig. 20 shows this design that must guarantee that the silicon substrate is exposed to the etching solution just where it is desired to accomplish the thin membrane (Marshall et al., 1992).

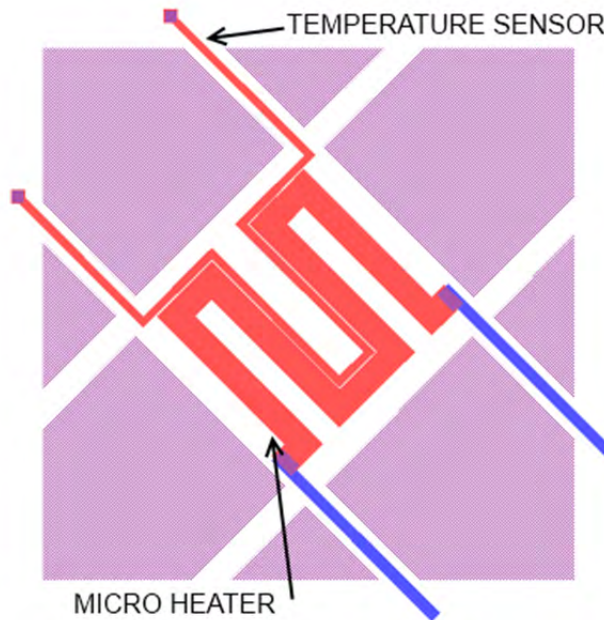


Fig. 20. Layout of micro-hotplate showing temperature sensor and micro-heater.

As mentioned before, this design is intended to be used in a CMOS semiconductor gas sensor that requires a heated thin film to perform the detection. Fabricating a micro-cavity below the heated zone using a MEMS etching process reduces the power needed to achieve the desired temperature and provides thermal isolation to the substrate and signal electronics (Suehle et al., 1993). This can be made following standard CMOS post-process etching steps, keeping compatibility between CMOS technology and MEMS micro-machining.

Using the guidelines explained before, it is expected that this design will help reduce damage to the exposed aluminium pads during the fabrication process due to the reduction of etching time.

6. Conclusions

It was theoretically and experimentally demonstrated that the geometry of a micro-hotplate (as the one used in CMOS compatible micro-heaters for semiconductor gas sensors) can be conveniently modified to reduce the etching time with TMAHW, in the order of 20%. Decreasing the etching time is notably useful if these structures are fabricated with materials that can be damaged by the etching solution used. Therefore, selective solutions with repeatability results should be used to protect the integrity of those layers that have an electrical or structural function and need to be protected during the post-process. The purpose is to keep these devices in the etching solution for the least possible time, protecting them from chemical damage. The geometry analysis proposed, based on crystallographic concepts, is a useful strategy in MEMS design taking advantage of anisotropic etching properties. For the cases here presented and using TMAHW, it is concluded that {111} planes and when possible the <110> directions that generate these planes, should be avoided not only in micro-hotplate membranes, but also in structures with different purposes, such as cantilevers. So, there is an optimization of the etching process, especially if it is included as a post-process for integrated circuits fabricated with CMOS technology compatible with MEMS technology.

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