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Basic readout circuit applied on FGMOS-based CMOS-MEMS inertial sensing prototypes

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Abstract – In this work is reported a brief summary of considerations for the design of a basic readout CMOS integrated system applied for the conditioning of small signals taken from a floating-gate based CMOS-MEMS capacitive structure intended for inertial measurement.

Both the electromechanical structure and the readout circuit (consisting in a variable capacitor coupled to the gate of a MOSFET and a conventional CMOS amplification stage, respectively) were designed for and fabricated in the 0.5um standard CMOS MPW platform available in ON Semi.

Simulation results for every component are presented as well as a comparison with measurements for the second stage of the readout system since the mobile capacitive structure (first stage) needs further post-processing to reach its proper functioning and desired behavior.

Keywords – CMOS-MEMS, FGMOS, MEMS, readout circuit, floating-gate, capacitive MEMS.

I. INTRODUCTION

Nowadays, microsystems dedicated to inertial sensing including accelerometers and gyroscopes are fully integrated within the architecture of several devices and systems ranging from entertainment to complex industrial and R&D applications. As shown in [1], [2] and [3], *floating-gate* MOS transistors have been successfully implemented as transduction mechanism when it comes to a CMOS-based MEMS device with a capacitive principle.

Floating-gate MOSFETs (FGMOS) have been typically used in non-volatile memory applications due to its particular electric charge storage properties. Since the so called "*floating*" terminal is embedded within dielectric oxides and therefore electrically isolated from the rest of the device, once the charge either positive or negative reaches this capacitively coupled instance it remains *trapped* until any high enough stimuli changes the amount of stored charge, usually through *Fowler-Nordheim tunneling* or *hot electrons* mechanisms. Is important to mention that up over the floating-gate terminal, there is a terminal commonly denominated *Control Gate*. The whole structure can be depicted as a capacitive voltage divider in which the floating-gate voltage (V_{FG}) is strongly dependent on the control gate voltage (V_{CG}) (Fig. 1).

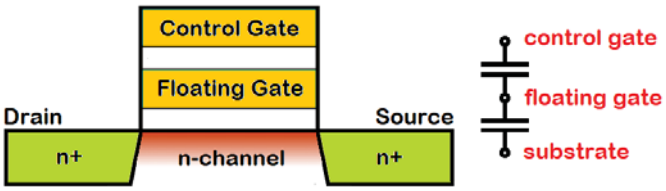

Fig. 1. FGMOS architecture and capacitive equivalent.

For the capacitive voltage divider shown above the relation between V_{FG} and V_{CG} is given by (1) where K is a proportional multiplier depending on the values of capacitance between the control gate and the floating gate and between the floating gate and substrate, C_Y and C_{ox} respectively, where the sub-indexes refers to the sensing structure (with free displacement in the Y-axis for a given application) and the oxide between the floating gate and the channel in the MOSFET conventional structure (2).

$$V_{FG} = K\,V_{CG} \tag{1}$$

$$K = \frac{C_Y}{C_{TOT}} = \frac{C_Y}{C_Y + C_{ox}} \tag{2}$$

Equations (1) and (2) models the DC behavior for a simple capacitive divider, nevertheless, for a dynamic floating voltage generation proportional to the inertial forces present at any time, we extend the model to a new one considering both the mobile parallel-plate capacitor (C_Y variable) and an additional control gate with an associated capacitance C_1 with the purpose of tuning an offset floating voltage if needed.

It is pointed out that two or more control gates over a single floating gate acts as an addition node for floating voltages as seen for two control gates in (3), one of them is variable and the other one fixed and following the architecture for the structure shown in Fig. 2.

$$V_{FG} = K_Y V_Y + K_1 V_1 = \frac{C_Y}{C_Y + C_1 + C_{ox}} V_Y + \frac{C_1}{C_Y + C_1 + C_{ox}} V_1 \tag{3}$$

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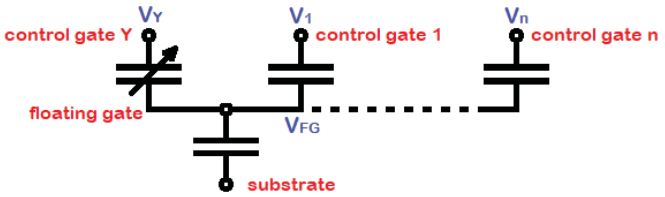

Fig. 2. Capacitive equivalent for the proposed structure.

The accelerometer studied in this work is reported in [4] and consist in a variable capacitor attached to a rectangular aluminum proof mass suspended by four spring anchored to the circuit substrate. The variable parallel-plate capacitor is mentioned to be a three-dimensional structure with a capacitance C_Y depending in the contributions of three planes in the form of (4), where Δy is the Y-axis displacement of the proof mass, n is the number of capacitive fingers in the array, ϵ_0 is the electric permittivity and the variables W, L, d and t are geometrical parameter specified in the same reference in compliance with [5].

$$C_Y = \frac{2 \cdot n \cdot \epsilon_0 \cdot W_f \cdot (L_f - \Delta y)}{d_{ox}} + \frac{(n-1) \cdot \epsilon_0 \cdot (t_{M1} + t_{M2} + t_{M3}) \cdot (L_f - \Delta y)}{d_{fin}} + \frac{n \cdot \epsilon_0 \cdot W_f \cdot (t_{M1} + t_{M2} + t_{M3})}{d_{tip} + \Delta y} \quad (4)$$

From previous simulations [4] in this work we consider C_Y to be fairly linear and ranging from about $5fF$ ($\sim 7.5fF$ neglecting some hanging in the Z-axis due to gravity) in a settle state to $\pm 1fF$ when the proof mass of the accelerometer is all the way displaced in the Y-axis.

II. SIGNAL CONDITIONING AND SIMULATION

Since the C_Y capacitance variations are very small, and so are the variations in the current driven within the transistor which dimensions are minimal, the electrical signal proportional to the acceleration must be conditioned in order to interact with external stages and devices. Most of commercial CMOS and MEMS-based sensors include either internal (monolithic) or external conditioning systems. As long as final signal is desired to be in the order of a few volts is usual to find many amplifier configurations regarding on the nature and origin of processed signals.

As seen in [6] fully differential amplifiers has proven compatibility for the readout of CMOS-based variable capacitor devices meeting minimal noise performance. Also, [7] describes a conditioning interface consisting in two stages, which improves gain and stability, also allowing to debug individual amplifier stages in simulations and measurements.

In this work, readout system is divided in two main stages, as seen in Fig. 3, the components for the first part are the floating-gate MOSFET with a variable capacitive structure coupled to the gate and a direct current to voltage transformation via a resistor in the drain terminal. The second stage is a common-source CMOS amplifier in the fashion of the one described in [8].

For the FGMOS device we arbitrarily selected a MOSFET with $L = 0.6\mu m$ (minimum channel length allowed by rules set in the $0.5\mu m$ technology) and $W = 6\mu m$ as we are not looking for a particular drain current specification but an easily readable, fairly linear voltage variation in the drain terminal (Fig. 4). A transistor with the dimensions described above would handle enough current so tuning a resistor R_1 in the order of $20k\Omega$ is expected to rise the drain node voltage to about 1V.

As expected in regular MOSFETS, when in saturation mode ($V_{DS} \geq V_{GS} - V_{TH}$), drain current I_{DS} will vary in terms of the gate voltage V_{GS}. For the FGMOS, the floating-gate voltage V_{FG} takes the place of V_{GS} as the driving voltage for the device and must be therefore along with V_{DS} greater than the threshold voltage V_{TH} at any time in spite of being a fraction of the voltage applied in the control gate denominated V_Y (Fig. 2) in this example. Fig. 5 shows the V_{DS}vsV_{FG} (V_{GS}) MOSFET characteristic in saturation ($V_{DD} = 3.3V, V_{TH} \cong 0.6V$) for many resistance values R in the setup seen above. R value is adjusted to approximately $23.3k\Omega$ (Fig. 6) in order to achieve a biasing of approximately $1V$ in the drain node when V_{FG} is also about $1V$ (less than a half the supply voltage). All the SPICE simulations ran over a set of parameters extracted from a previous fabrication process.

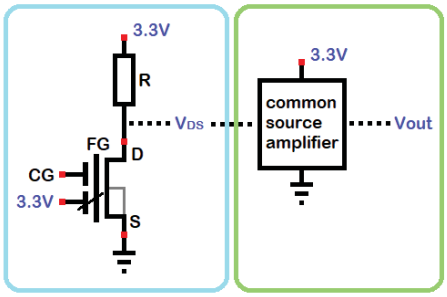

Fig. 3. Two-stage readout circuit.

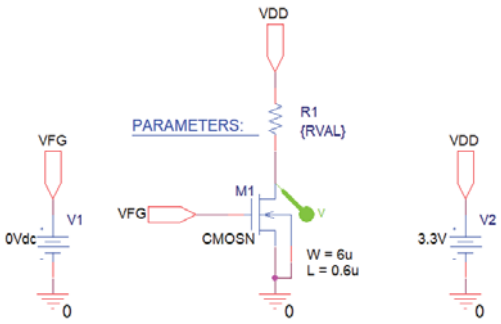

Fig. 4. First stage simulation setup.

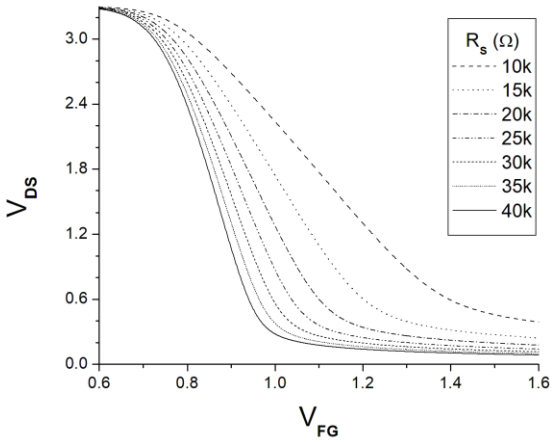

Fig. 5. R value sweep looking for a suitable biasing in drain node.

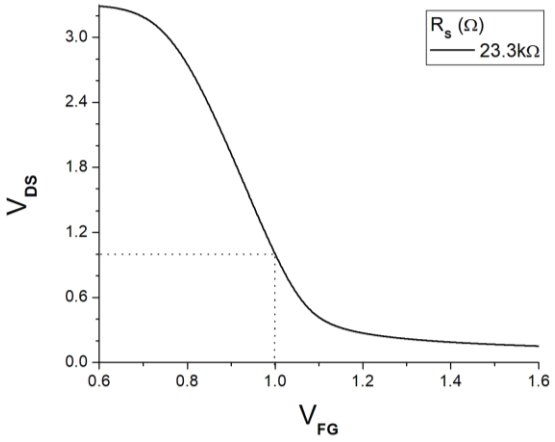

Fig. 6. Selected VDS characteristic.

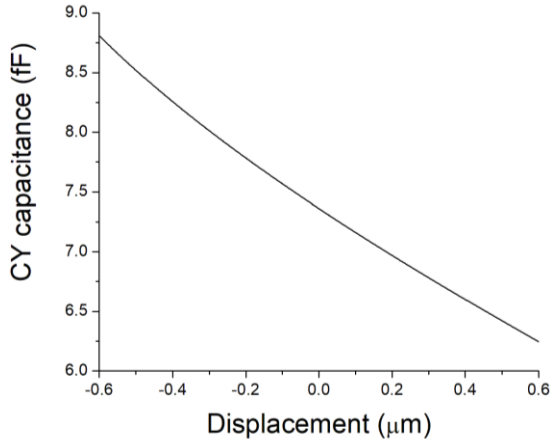

Fig. 7. Capacitance variations according to displacement.

At this point, we recall the changes of capacitance C_Y in the variable capacitor according to the displacement in the proof mass of the accelerometer. As seen in equation (4) C_Y has two linear and one non-linear terms, being the latter the lowest contribution. Fig. 7 and Fig. 8 show respectively the discussed capacitance and the consequently variation in the floating-gate potential according to equation (3) when V_{CG} (V_1) is tuned to $0.879V$ (looking for a $1V$ capacitively coupled voltage in the floating terminal when the displacement is zero).

Is important to notice that the function of the control gate is to offset the voltage induced in the floating terminal as it works as an (neuromorphic) addition node. The iterative evaluation of equation (3) searching for a suitable V_1 was performed in Matlab.

After evaluating the floating potential for a given list of possible displacement values we may obtain a text file that can be feed to a file-controlled voltage source in the PSPICE simulation environment. Fig. 9 and Fig. 10 represent respectively the schematic setup including a floating gate voltage input via a text file from previous capacitive simulations and the resulting V_{DS}vsV_{FG} characteristic.

This characteristic (Fig. 10) appears to be a bit less linear than the variation in V_{FG} (Fig. 8) but this may be actually an effect of the amplification factor for the first stage. As can be extracted from the simulations, variation in the floating potential (not perfectly symmetrical) goes, let's say, $30mV$ around the $1V$ biasing at zero displacement, while V_{DS} reaches about $300mV$ below or above its own $1V$ initial point at maximum displacement. $\Delta y = 0.6\mu m$ is the maximum deflection in the springs holding up the proof mass and corresponds mechanically to an acceleration about 8 times greater than the gravity's $(8G)$ in the proposed accelerometer.

Summarizing for the first stage of the readout system, having specifications such as the displacement in the proof mass, the supply voltage and equations (3) and (4) we obtain the voltage characteristic in the floating terminal, noticing this potential is capacitively coupled as in voltage dividers so the charge trapped within the floating gate is desirable zero and has no threshold shifting effects unlike the typical charge storage applications of the FGMOS. Then, a list of MATLAB simulated corresponding V_{FG} values is used to simulate and perform a fine tuning of R and V_1 obtaining a new list of PSPICE simulated V_{DS} values.

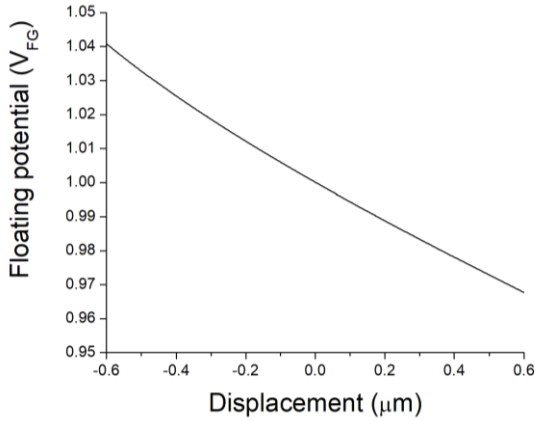

Fig. 8. Capacitively coupled floating-gate voltage variations.

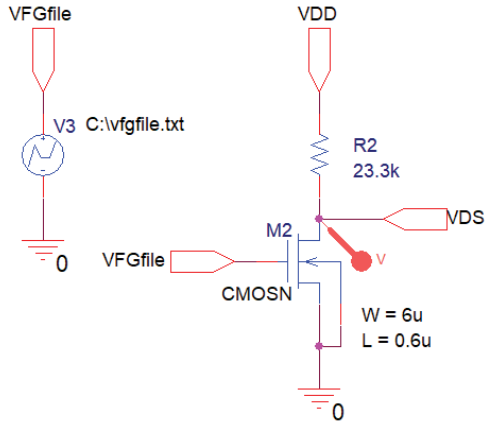

Fig. 9. Setup for a VDS simulation with non-linear previously-simulated floating-gate voltages.

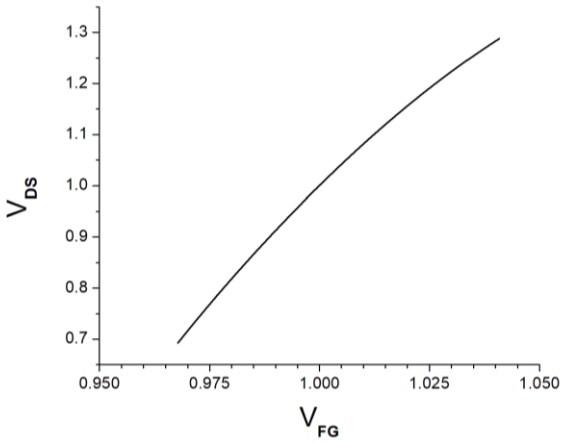

Fig. 10. VDS node voltages as floating gate potential varies.

Second stage consist in a common-source amplifier which is actually formed by four conventional MOS transistors. This architecture was selected over differential and cascade amplifiers due to its simplicity and ease to achieve a fairly linear quite large region by the adjustment of a few parameters in biasing transistors. Setup for the electrical simulation (Fig. 11) includes one more file-controlled voltage source, this time controlled by the data text file extracted from the previous V_{DS} simulation.

The dimensions W and L for both PMOS transistors (on top) and the NMOS output transistor (bottom right) were firstly arbitrarily proposed and the NMOS in the bottom left (in diode mode for biasing purposes) was tuned in order to pull the linear transition of the characteristic output curve (Fig. 12) near to the $1V$ steady-state output of the previous stage. Finally, the dimensions of the output PMOS (top right) are iteratively adjusted along with the biasing NMOS transistor ensuring the largest linear region possible looking for more gain in the overall performance.

The characteristic in Fig. 12 is the output for the second stage in a DC sweep with a full-range input within the supply voltage (selected to be $3.3V$ in order to comply with most unitary lithium polymer cells, commonly used in portable and embedded systems). Signals from previous stages are intended to oscillate around the $1V$ voltage and fit within the linear transition region of the inverter-alike common-source amplifier implemented.

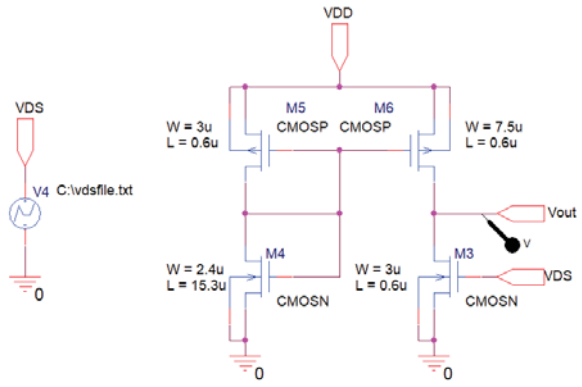

Fig. 11. Second stage simulation setup.

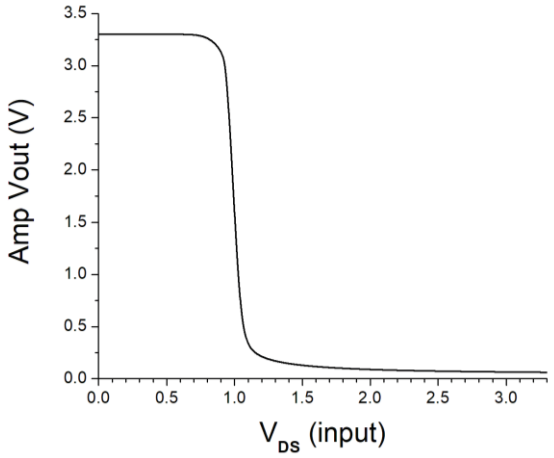

Fig. 12. Simulated output for the common-source amplifier.

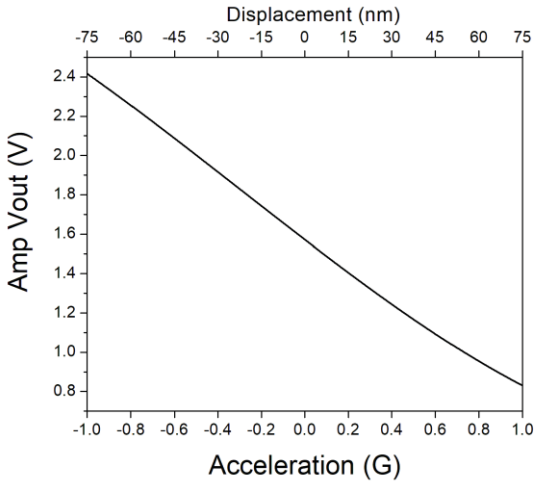

Fig. 13. Output (easy-readable) voltage vs acceleration.

The overall performance of the system following the *displacement* → *capacitance* C_Y → *FGMOS current* I_D → *FGMOS voltage* V_D → *amplied output* V_{out} path is shown in Fig. 13. As seen above, for $1G$ (gravitational acceleration) which correspond to a displacement of about $75nm$ in the Y-axis of the proof mass, the output voltage is near to $0.80V$ over the zero displacement (zero acceleration) output (~1.6V). Simulated drain current in biasing transistors M4 and M5 is about $10\mu A$, quite normal to transistor this size but also susceptible to further improvement in energy management issues.

III. MEASUREMENTS

Since the $0.5\mu m$ conventional CMOS process is not MEMS-compatible a rigorous chemical wet post-processing must be applied on the chip in order to release the mechanical structures that enables the proof mass, this process haven't been optimized to the date. However, the common-source amplifier (second stage) was designed to be tested in a standalone setup having access to most of its nodes from the exterior pad bonds.

The layout (Fig. 14) for the common-source amplifier includes both the FGMOS and the common-source amplifier. The first stage (left) features connection to the movable structure and the offset control gate, for the second stages, PMOS transistors (center) and NMOS transistor are conFig.s as in Fig. 11, having an special arrangement for the biasing diode-mode transistor which is very large in its L value (channel length), so it is replaced with four shorter transistors in series connection with a combined effect similar to the characteristic in Fig. 12.

A measurement of the fabricated cell shown in Fig. 14 is presented in Fig. 15, based on the results from Fig. 13 is fair enough to state that the linear behavior is preserved for the same output range ($approx. 0.8\ to\ 2.4V$). The (almost) linear region in the I-V characteristic for the actual amplifier is shifted about $150mV$ in the horizontal axis maybe as a result of neglected parasitic capacitances or some mismatches in simulated model considering that one of the transistors with a large L parameter was replaced by four series smaller transistors in order to fit design areas. This shift might be corrected slightly changing the biasing in control gate for the first stage, further simulation and a wider characterization for the second stage must be performed.

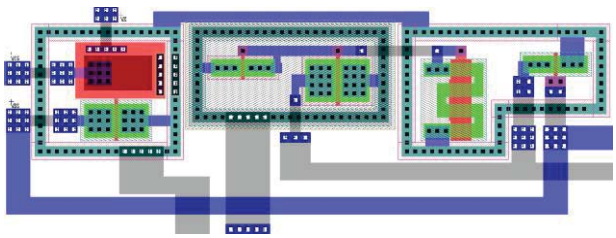

Fig. 14. FGMOS and common-source amplifier layout.

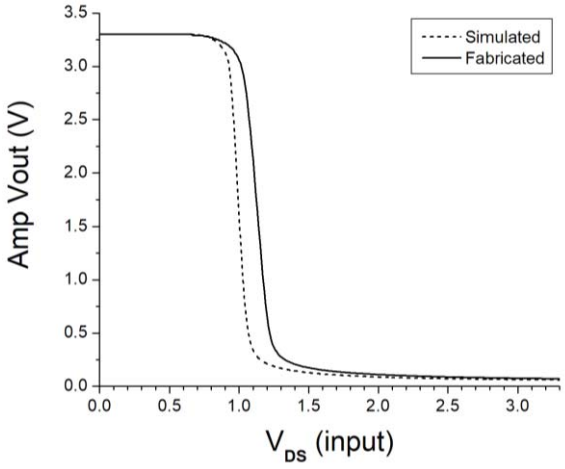

Fig. 15. Simulated vs fabricated output curves.

IV. CONCLUSIONS

The readout system designed following the procedure reported in this work is suitable for full integration with other on-chip and discrete components as its overall sensitivity is estimated in $0.8V/G$, featuring a relatively high voltage output within a range of relatively low accelerations.

As expected, a complete system involving movable part, capacitive couplers, transducing FGMOS transistors and analog signal conditioners is suitable to be monolithically fabricated and tested. A single-chip prototype insures lower costs and easier measurement setups enhancing the capabilities of the device to be integrated into larger embedded systems.

It is important to keep the MOSFET in saturation mode and therefore is needed to choose capacitive values so the floating gate voltage V_{FG} remains greater than the threshold voltage V_{TH} after applying the K coupling factor and the relation $V_{DS} \geq V_{GS} - V_{TH}$ is satisfied.

Although there is a unneglectable displacement between curves for the simulated and measured second stage amplifier, they have fairly the same behavior and change the value of some tuning bias voltages may correct the operation points of both stages in the system with very small affectation in the linearly of the response.

Promising results in the analog domain encourages to continue the development of inertial FGMOS-based micro systems, looking forward to digital high signal-to-noise relation circuits.

V. FUTURE WORK

Propose new or apply proprietary automation mechanisms in the circuit design and location of operation points for every component across the two stages improving the system's overall performance.

Verify the source of mismatch between the designed/simulated and fabricated/measured amplifiers, the error gap might have one or multiple origins including undesired charge trapped in the fabrication process, models and simulation parameters out of date (and newer ones protected by intellectual property statements), among others.

Residual trapped charge from the fabrication process might be removed by exposure to ultra-violet light or prevented following the discharge mechanism described in [9] where a discharge path is always available for the floating gate during the deposition and etching fabrication processes.

Optimize power consumption and management in order to improve the autonomy in mobile and embedded applications.

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