A Very Low Offset Voltage Operational Amplifier Using Field Programmable Floating-Gate Technology

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Abstract

A very low offset voltage operational amplifier that can be field programmable is described. Offset reduction is achieved by programming two floating gate transistors that form an important part of a single-stage folded cascode amplifier. A novel programming method that requires just four additional pins and an LMS algorithm was used. Floating-gate transistors were programmed for a minimum offset voltage of ±20μV using 1.2μm CMOS process. Programmed operational amplifiers can be used in continuous-time operation for a long period of time without the need of reprogramming. Experimental results show that this offset reduction scheme is a viable approach to low cost precision operational amplifier fabrication.

1. Introduction

An operational amplifier is an important block that is extensively used in analog and mixed-signal circuits. Many of these circuits require special characteristics from the operational amplifier such as low power consumption and low input-referred offset voltage. The first characteristic is easy to obtain if CMOS process is used, the second characteristic is nowadays a challenge for analog circuit designers due to mismatch. Mismatch represents a serious design problem caused by non-perfect symmetry of MOS transistors, it means that two or more transistors that are designed with the same geometry relation (W/L), are not exactly equal due to technological parameter variations and fabrication imperfections [1], [2], [3].

Techniques commonly used to reduce the offset voltage in operational amplifiers include auto-zeroing, correlated double sampling and chopper stabilization [4]. Another commonly used technique include using laser trims, however it is expensive. Some commercial amplifiers like OP177 are factory adjusted using this technique.

In this paper a continuous-operation ±20μV offset voltage operational amplifier is presented. Mismatch effects over DC offset are cancelled using two currents sources (floating-gate transistors) that are trimmed by an off chip digital circuit that is cheaper than a laser trimming machine making this a real low cost field programmer.

Programming is achieved by using LMS algorithm that determines the frequency of the pulses that are applied to the injection terminal of each floating-gate transistor [5]. Indirect programming is used to avoid the need of analog switches [6]. This novel programming technique does require neither internal switches nor additional terminals for controlling them.

In section 2, common offset reduction techniques are discussed including floating-gate current source trimming. In section 3, electron tunneling and hot-electron injection mechanisms for controlling the floating-gate charge are presented. The indirect programming advantages over direct programming are also presented. Section 4 describes a novel field programming off chip circuit that utilizes an LMS block as the main part. Programming process implementation is also described. In section 5, a precision folded-cascode amplifier with two trimming current sources for cancelling offset voltage is described. In section 6, experimental results obtained from the precision amplifier are compared with a non-trimmed version of the same amplifier, showing the real advantages of this circuit. Finally, section 7 concludes by summarizing the experimental results obtained.

2. Offset cancellation

In this paper the term "offset cancellation" is used to describe an operational amplifier with an input referred offset voltage less than 100μV. This

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operational amplifier is commonly call "precision amplifier"

Many offset cancellation techniques have been reported, the most common are: autozeroing (AZ), correlated double sampling (CDS) and chopper stabilization (CHS). AZ idea is sampling the unwanted offset and subtracting it from the instantaneous value of the contaminated signal either at the input or the output of the amplifier. CDS implies two sampling operations: a first one to sample the offset, followed by a second sampling of the signal. CHS applies modulation to transpose the signal to a higher frequency and then demodulates it back to the baseband after amplification [4].

2.1 Floating-gate current source trimming

Another offset reduction technique for operational amplifiers is presented in [7]. This technique implies two trimming current sources that are connected at the folded-cascode output networks in order to equal the currents when both amplifier inputs are at the same potential.

The equivalent circuit is shown in Figure 1. Trimming current sources represented by I_t, compensate the error output current caused by the input-referred offset voltage V_{OS}.

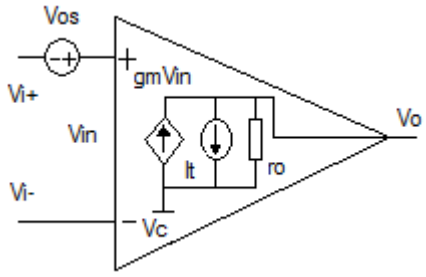


Figure 1. The equivalent circuit for a precision amplifier using the trimming current technique. Vin is the input signal and is equal to V_{I+} - V_{I-}, gmVin is the output response that is affected by the input referred offset V_{OS} and r_0 is the amplifier output resistance.

The input referred offset voltage is caused by mismatch effects on the geometry relation and threshold voltage. For a differential pair which is one of the most important parts of an operational amplifier, the input referred offset voltage is:

$$V_{OS} = \frac{V_{GS}-V_{TH}}{2}\left(\frac{\Delta(\frac{W}{L})}{(\frac{W}{L})}\right) - \Delta V_{TH} \qquad (1)$$

Where $\Delta(W/L)$ is the geometry relation mismatch ΔV_{TH} is the threshold voltage mismatch, and V_{GS} is the gate-source voltage of the differential pair transistors. In section 3 the floating gate charge is used to control the threshold voltage of the transistor making this device ideal for ΔV_{TH} compensation.

3. Floating Gate MOS Transistor for indirect programming

A floating gate is a polysilicon gate surrounded by SiO_2. Charge on the floating gate is stored permanently, providing a long-term analog memory, because it is completely surrounded by a high-quality insulator. Figure 2 shows a p-channel floating gate MOS transistor layout that is primary used for indirect programming.

Floating gate charge is controlled by two physic mechanisms: tunneling and hot electron injection [8], [9].

Tunneling removes electrons from the floating gate. An electric field across the oxide will result in a thinner barrier to the electrons on the floating gate. For a high enough electric field, the electrons can tunnel through the oxide. The functional form of tunneling is:

$$I_{TUN} = I_{0TUN} e^{-\frac{t_{ox}\xi_{ox}}{V_{TUN}-V_{FG}}} \qquad (2)$$

Where I_0 is the pre-exponential current, t_{ox} is the gate-oxide thickness, V_{TUN} is the tunneling voltage, V_{FG} is the floating gate voltage and ξ_{ox} is a constant with a value of 25.6V/nm. From equation (2) is shown that tunneling current increases exponentially with the difference between V_{TUN} and V_{FG}.

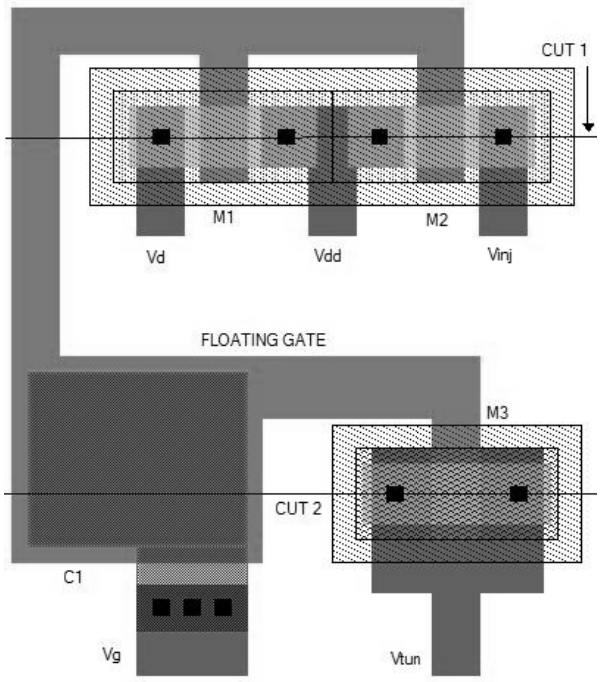
Hot electron injection adds charge to the floating gate. The physics of the injection process is to give some electrons enough energy and direction in the channel to the drain depletion region to surmount the SiO_2 energy barrier [10].

The injection current can be approximated as:

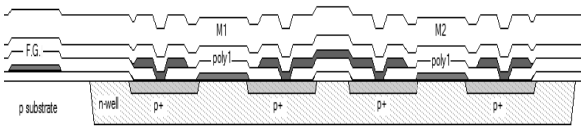
$$I_{INJ} = -I_S e^{f(V_{d-c})} \qquad (3)$$

Where V_{d-c} is the voltage from the drain to the drain edge of the channel, then injection current increases exponentially with the drain to source voltage

Tunneling and hot electron injection is used to program the floating gate transistors of the operational amplifier.



(a)



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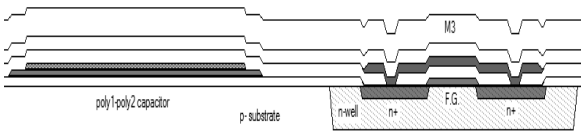

(c)

Figure 2. Geometry design of a p-channel floating gate transistor (FGMOSFET). (a). Layout of a FGMOSFET used for indirect programming. Note that there are two pfets, one is the principal p transistor and the other serves as an injection structure. (b). Transversal view of cut1 showing two pfets. (c). Transversal view of cut2 showing the control gate capacitor formed between poly1 and poly2 and the tunneling structure.

4. Field Programming

Field programming is a practical and low cost method to program floating gate transistor. In [7] and [11], a field programming method is used. In [7] the programming process requires several internal switches to perform the program function. In this paper a novel field programming method that utilizes indirect programming to avoid the use of internal switches is presented.

Figure 3 describes the principal blocks of the hardware used to perform field programming.

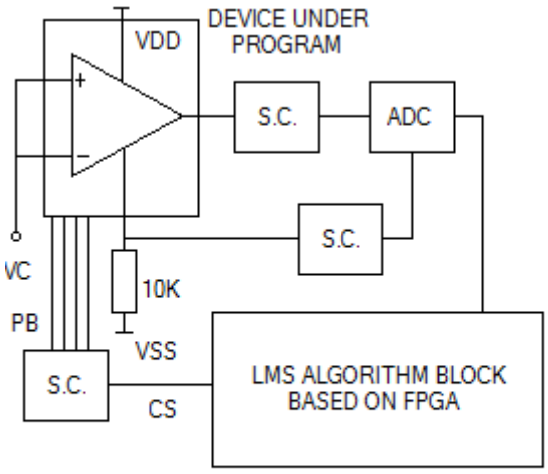

Figure 3. Block diagram of the field programmer. The device under program is connected as follows: its inputs are shorted and driven to a common voltage V_C that is 2.5V, V_{DD} pin is connected to a D.C. source of 5V and V_{OUT} and V_{SS} are connected in such way that it is possible to read the output voltage of the amplifier and the consumption current. The field programmer needs three signal conditioners, one analog to digital converter and a FPGA to perform the computational algorithm.

As shown in Figure 3, supplied current and output voltage of the amplifier is sampled by an ADC in order to send these data to the FPGA that will process and generate the adequate pulse frequency in the injection pins.

For a 1.2µm CMOS process, tunneling voltage must be around 27V. Due to the high tunneling voltage, this mechanism is used just as an erase signal. Hot electron injection is used to perform the programming process. Hot electron injection instead of using a great voltage around 27V, it requires only 7.5V between drain to source pins.

The programming process is as follows:

a. The Operational amplifier must be supplied with 5V and its inputs must be short-circuited and held to 2.5VDC that is the reference voltage.
b. The system erases the floating gate transistors by tunneling, applying 27V on V_{TUN} terminal.

c. System reads the supplied current and start injecting one of the floating gate transistors connected to the output network of the folded cascode until the current approximately reaches 8μA that is the current calculated in theory.
d. System continues reading the supplied current and start injecting the second floating gate transistor until the current reaches 16μA, the double of one tail current. By this time the floating gate voltages are around 3.87V and a minimum of ΔV_{FG} is required for offset cancellation. This short variation of V_{FG} lets the system to use an LMS algorithm due to the linear dependence approximation of V_{FG} due to V_{inj}.
e. System then start reading the output voltage that must be around 2.5V and perform an LMS algorithm to calculate the frequency of the pulses applied in both injection pins until the output reaches 2.5V as closed as possible [5], [12].
f. The resolution of the system depends on the minimum duration of the injection pulses.

This process is represented in Figure 4.V_G and V_{DS} are polarization voltages necessary to perform either tunneling or electron injection. V_{TUN} is used to erase the floating gate transistors at the very first beginning and is not used to perform LMS algorithm.

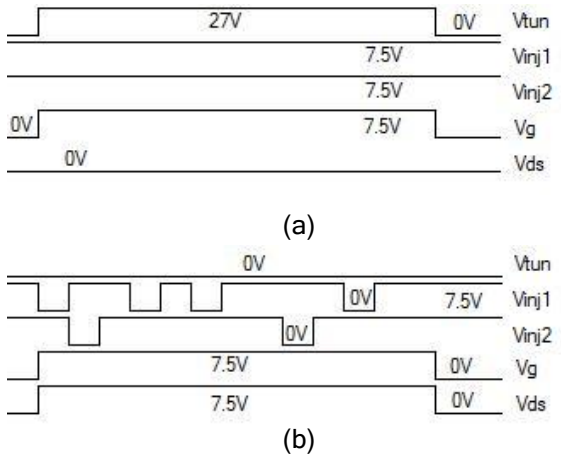

Figure 4. The graphical representation of the programming process. (a). The erasing process. This process sets the cascode current to zero. (b). The programming process. The pulses in V_{inj1} and V_{inj2} vary their frequency according to an LMS algorithm.

4.1 The LMS Algorithm

The least mean square algorithm uses a gradient descent method to update the weights of a linear filter or neural network. Equation (4) describes the basis of the LMS algorithm that is computed by the FPGA.

$$w_i(n+1) = w_i(n) + \gamma x_i(n) e(n) \qquad (4)$$

Where w_i is the weight or the floating-gate voltage on each transistor, γ is the adaptation rate, x_i is the voltage at the input of the LMS block which is the operational amplifier output voltage and e is the error at the operational amplifier output V_{OFF}

LMS algorithm was implemented to perform the offset cancellation as follows:

First, the input referred offset voltage can be obtained from V_{OUT} (Operational Amplifier Output voltage) if we short-circuit the inputs and tied them to a reference voltage V_{REF}. Equation (5) shows this relation.

$$V_{IROV} = \frac{V_{OFF}}{AV} \qquad (5)$$

Where V_{OFF} is the output offset voltage and is equal to V_{REF} -V_{OUT} and AV is the open loop gain.

The output offset voltage V_{OFF} depends on the symmetry of the two output tails of the folded-cascode circuit. This symmetry is affected by mismatch, but as shown in Figure 1, the mismatch can be compensated by adding a programmable current source I_t on each folded-cascode tail. The circuit on Figure 5 was implemented. BL1 and BL2 are the floating-gate transistors that work in the saturation region. The drain current of a p-channel floating-gate transistors in saturation is:

$$I_D = \frac{1}{2}\mu_p C_{ox} \frac{W}{L} (|V_{DD} - V_{FG}| - |V_{TH}|)^2 \qquad (6)$$

Where μ_p is the mobility, C_{ox} is the gate-oxide thickness, V_{TH} is the threshold voltage and V_{FG} is the floating-gate voltage that is:

$$V_{FG} = w_i = \frac{Q_{FG}}{C_T} \qquad (7)$$

Where Q_{FG} is the total charge in the floating gate and C_T is the total capacitance seen by the floating gate. Assuming that C_T and V_G are constant, the voltage variation on the floating gate ΔV_{FG} depends on the floating gate charge Q_{FG} only. This charge is controlled by the two mechanisms described in chapter 3.

Simulations and experimental results show that if we have a certain floating gate voltage and we want to change this voltage less than 200mV; the floating gate voltage has a linear dependence on V_{inj} and V_{TUN}. This is very helpful because LMS can be used with no problems.

LMS algorithm uses hot electron injection only, so the sign of the error is achieved by selecting BL1 or BL2 to be injected. In our design V_{inj} was frequency encoded in order to avoid the use of complex hardware and to reduce noise interference.

To summarized LMS implementation, steps (a) to (d) of the system programming procedure must be done to prepare the floating gate transistor to be programmed using a ΔV_{FG}<200mV. If this condition is true V_{FG} is:

$$\Delta V_{FG} = \alpha V_{inj} \quad (8)$$

Where α is a constant and V_{inj} that is used in the programming process shown in Figure 4(a) is related with V_{OFF} with equations (6), (7) and (8).

5. Folded-Cascode Architecture

Our circuit employs folded cascode architecture with output buffer. Figure 5 shows the electric diagram of the operational amplifier.

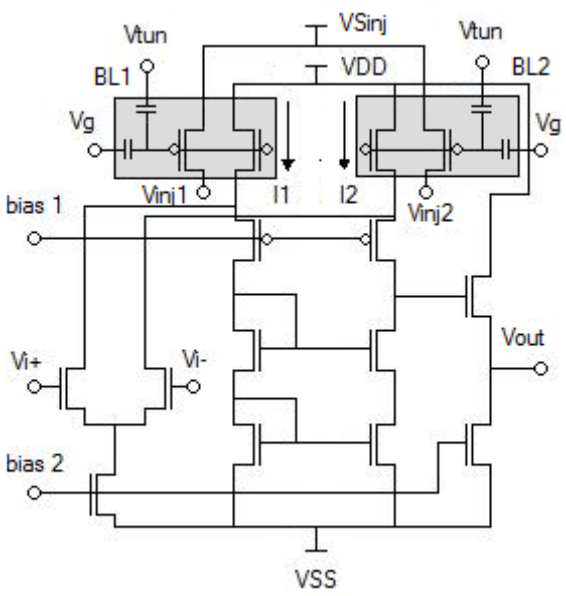

Figure 5. Folded cascode operational amplifier. BL1 and BL2 are floating gate transistors that are indirect programmed.

Layout of the folded cascode amplifier is shown in Figure 6. This design can be easily scaled to submicron technologies. Tunneling and Injection voltages will decrease.

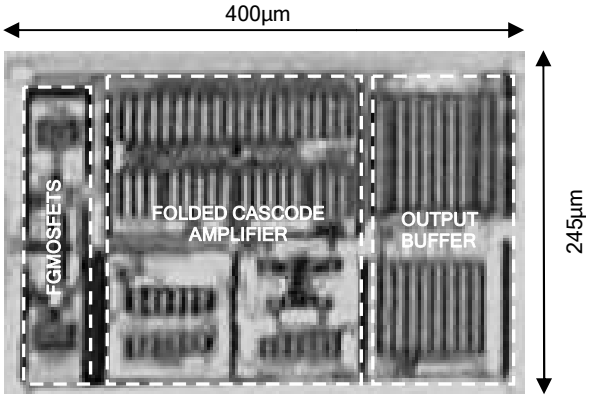

Figure 6. The chip micrograph of the precision amplifier. The total area including output buffer is 400µm x 245µm using 1.2µm technology. The offset cancelled folded cascode requires 15.6% more die area to implement FGMOSFETs.

6. Experimental Results

Several characterization tests were made to the operational amplifiers. It was designed on chip two different folded-cascode amplifiers, the first one correspond to a simple operational amplifier, the second one correspond to a very low offset voltage operational amplifier using the floating gate trimming technique.

Table 1 shows the experimental results obtained from the simple folded-cascode. Table 2 shows the experimental results obtained from the low offset voltage operational amplifier after a successful programming.

The unity gain bandwidth was dramatically reduced because the need of very high stability >70º, reducing the phase margin at 60º will increase the unity bandwidth up to 10 MHz.

Results show a very large difference in offset voltage parameter, that is the main goal of this offset reduction technique. Floating gate trimming technique in combination with indirect programming result in a very viable approach to offset cancellation and a very low cost production option compared with the current laser trimming technique.

Table 1. Experimental results obtained from a simple folded-cascode operational amplifier.

Parameter	Value
Supply voltage	5V
Technology	1.2µm
Input Offset Voltage (minimum)	4mV
Open loop gain	64.5dB
Unity Gain Bandwidth	233khz
Phase Margin	70º
Common Mode Rejection Radio	65dB
Power Supply rejection Radio	70dB
Slew Rate	2V/µs
Total power dissipation (with buffer)	12.3mW

Table 2. Experimental results obtained from a floating gate trimming folded-cascode operational amplifier.

Parameter	Value
Supply voltage	5V
Technology	1.2µm
Input Offset Voltage (minimum)	20µV
Open loop gain	65dB
Unity Gain Bandwidth	235khz
Phase Margin	70º
Common Mode Rejection Radio	65dB
Power Supply rejection Radio	70dB
Slew Rate	2V/µs
Total power dissipation (with buffer)	12.3mW

7. Conclusion

A novel offset reduction technique was presented. The experimental results show a new viable approach to offset reduction. The operational amplifier described in this paper meets the requirements to be used in high accuracy equipment. This technique can reduce offset voltage up to 20µV that is less than the mayor commercial precision operational amplifiers.

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