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Behavioral Modeling of a Sigma-Delta Modulator for Sensing Photocurrent in a CMOS Image Sensor

S. Garduza-González[1], F. Gómez-Castañeda[2], V. H. Ponce-Ponce[3], and J. A. Moreno-Cadenas[4]
[1]Interdisciplinary Professional Unit on Advanced Engineering and Technology (UPIITA)
[1,2,4]Research and Advanced Studies Center (CINVESTAV), [3]CIC, all of the National Polytechnic Institute (IPN)
Mexico City, Mexico
Phone (+5255) 5747-3800 E-mail: [1]sgarduza@ipn.mx, [2]fgomez@cinvestav.mx, [3]vponce@cic.ipn.mx

Abstract—**We propose behavioral time-domain modeling for a Sigma-Delta Modulator (ΣΔM) to sense photocurrent in a CMOS Image Sensor (CIS). The model starts from transfer function for first-order single-bit ΣΔM in discrete-time, and then adds noise sources and nonlinearities by introducing noise floor and harmonic distortion, which determine system performance. The results were compared with the measurements of a CIS based ΣΔM circuit prototype fabricated with CMOS technology. The model showed good agreement with measurements.**

Keywords—**Sigma-Delta modulator, CMOS image sensor, behavioral modeling, passive pixel sensor.**

I. Introduction

Since their invention, the CMOS Image Sensors (CIS) have evolved in reading speed (frames/s), dynamic range, and pixels density, but these issues do not draw any advantage if they are not accompanied by a high-performance ADC, either for immediate visualization of the image or for on- or off-chip post-processing.

The ΣΔM based ADC belongs to the group of oversampling converters, which means that, unlike converters based on Nyquist's frequency (f_{Ny}), it can filter temporal noise (noise shaping) without using low pass filters [1], thus requiring a smaller area. Less noise means the Signal-to-Noise Ratio (SNR) is increased, accepting likewise a more dynamic range of the input signal (DR_{signal}). Nevertheless, a larger DR_{signal} can lead to nonlinearities in the circuits. The ΣΔM ADC, given its characteristics and settings which are not as accurate (as would be for Nyquist's converter), supports a range of nonlinearities and thus achieves a specified SNR. These properties make the ΣΔM ADC a suitable choice for the CIS design. According to above, in a CIS, the ADC can be an implemented circuit: pixel, column or chip level. Intermediate performance can be reached by taking the SNR and speed at column level into account.

The SNR is the standard parameter for measuring the ADC performance, but it becomes a problem if there are no analytical expressions developed. Such expressions must contain temporal noise sources that degrade the performance. A good strategy is to consider the main effects that influence the performance and developed their behavioral model. This methodology has been used as a design rule for the design of these systems [2], [3]. This work presents behavioral time-domain modeling for a first-order single-bit ΣΔM embedded in a CIS. The model was developed with Simulink™ in Matlab™ and includes real noise sources. The nonlinearity from the light sources is considered, then we add floor noise and harmonic distortion to the model. The results were validated against actual measurements.

II. Background

A first-order single-bit ΣΔM discrete-time system consists of an integrator, a quantifier and feedback. If the system meets certain conditions [4], the quantifier is modeled as an additive white noise source with variance $\overline{e_q^2}$ (in V^2/Hz), and its power spectral density (PSD) $N_{eq}(f)$ is:

$$N_{eq}(f) = \frac{\overline{e_q^2}}{f_s} = \frac{\Delta^2/12}{f_s} \tag{1}$$

Where Δ is the quantification step and f_s is the sampling frequency. In an ADC, with oversampling rate R, the $f_s = R \times f_{Ny}$ and f_{Ny} is the Nyquist's frequency. Thus, the initial transference function is:

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)E(z) \tag{2}$$

Where $\left(z^{-1}\right)$ is the signal transfer function (STF) and $\left(1 - z^{-1}\right)$ is the noise transfer function (NTF). As the quantification noise $E(z)$ is the only source included in (2), the signal to quantification noise ratio (SQNR) will be the "idealized" reference parameter.

The SQNR is defined as the ratio of the signal power to the quantification noise power [5], i. e. $SQNR = P_{signal}/P_{eq}$. Analytically P_{eq} is calculated by integrating the magnitude of NTF modulated by $N_{eq}(f)$ in the bandwidth (BW) of interest.

$$P_{eq} = \int_{-f_b}^{f_b} |NTF|^2 N_{eq}(f)\, df = \overline{e_q^2}\frac{\pi^2}{3 \cdot R^3} \tag{3}$$

If we take the digitalization of sinusoidal signal, with peak voltage V_p, the power is $\overline{v^2} = V_p^2/2$. Then, the obtained SQNR is:

$$SQNR = \frac{18 \cdot R^3 V_P^2}{\pi^2 \Delta^2} \tag{4}$$

III. CMOS Image Sensor Architecture

The test CMOS Image Sensor is a prototype designed to capture still images in gray scale, and consists of a matrix chip with 24×24 passive pixels sensor (PPS), using p-diffusion/n-well photodiode. The DR_{signal} was determined by the physical structure and size of the photodiode, in which we measured from $50\,\mathrm{pA}$ to $100\,\mathrm{nA}$, covering a wide range of light intensity. The rows were selected by the shift register and every four

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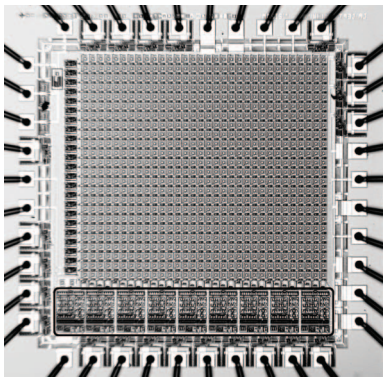

Fig. 1. Prototype CIS microphotography with 9 ΣΔM column level and row-column selector.

columns share a ΣΔM through 4×1 analog MUX. In addition, there is a test circuit ΣΔM making total of 9 ΣΔM similar circuits. The CIS based ΣΔM prototype was fabricated with $1.2\,\mu$m CMOS technology. A microphotography is shown in Fig. 1. The 9 ΣΔM are enclosed in a rectangle.

The basic cell is formed by a PPS (signal source), a row/column switch and the ΣΔM, as models (2) and shown in Fig. 2. Conventionally, the integrator is formed by switch-capacitor common-mode feedback [1] since the circuits have a high output swing, high accuracy and low static power consumption, but the circuits occupy a large area of Si. A differential-pair (diff-pair) elemental was chosen and the specification obtained from Spice simulation, are summarized in the Table I. The quantifier is a clocked comparator. A switched-capacitor (SC) circuit works in the feedback as proposed in [6]. The SC circuit carries out the Digital/Analog Converter function. No need a hold capacitor, since the signal to convert (photocurrent) is coming directly from the photodiode.

The test cell is, randomly, selected to estimate the performance. A beam of light from the LED is incident on the photodiode active surface. This beam is modulated by a sinusoidal function with amplitude and frequency like in (6). The test frequency is $BW = 7.81\,\text{Hz}$, $R = 64$ y $f_s = 1\,\text{kHz}$. For a modulated power with $V_p = -3\,\text{dB}$ ($V_{ref} = 1\,\text{V}$), using (4), is obtained $59.8\,\text{dB}$ of SQNR. Model (2) was implemented in Simulink™ and simulated 16 input signal cycles. The output signal in time-domain is Pulse Code Modulation (PCM) type and we calculated the PSD with 4096 samples, finally obtaining $59.4\,\text{dB}$ of SQNR. This value is very close to that given by (4). For digital still cameras the exposure time determines the speed sensor readings, generally are between $30\,\text{s}$ and $1/3\,000\,\text{s}$. $BW = 7.81\,\text{Hz}$ frequency signals allow a exposure time of about $1/8\,\text{s}$.

Once the "ideal" situation has been modeled, we added no correlated noise sources to the Simulink™ model in order to obtain noise floor power (P_{NF}) and harmonic distortion power (P_{HD}). We were then able to obtain the Signal-to-Noise and Distortion Ratio (SNDR):

$$SNDR = P_{signal}/\left(P_{eq} + P_{NF} + P_{HD}\right) \tag{5}$$

TABLE I
INTEGRATOR SPECIFICATIOS

B	Integrator coefficient	0.3
C_s	Capacitor	20 fF
SR	Slew-Rate	$1\,\text{V}/\mu\text{s}$
$UGBW$	Unity gain bandwidth	5 MHz
A_{OL}	Open-loop gain	48.8 dB
V_{sat}	Saturation voltage	1.5 V
ΔV_{out}	Range of diff-pair output voltage	30 mV

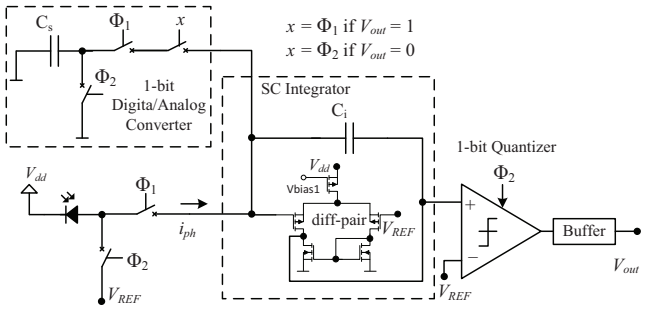

Fig. 2. Electrical circuit of the first-order ΣΔM implemented to column level on CIS.

The considered noise sources are modeled in the next section.

IV. Behavioral Modeling of Noise Sources

A. Nonlinearity and noise of the light source

The device used to characterize the CIS performance is a LED, whose emitted photon flux density has an incident optical power (p_{ph}, in W/cm^2) and wavelength spectrum (λ, in nm). White light LED was used for our characterization, biased at an operating point, and modulated signal was added. The power p_{ph} is:

$$p_{ph}\left(t\right) = P_{ph0} + MP_{ph0}\sin\omega_0 t \tag{6}$$

Where ω_0, M and P_{ph0} are the deterministic signal angular frequency, the modulation factor and the incident optical power at bias point, respectively. This power is modified by the signal jitter noise and device nonlinearity. In regard to the jitter noise signal, we assume that the excitation signal is displaced by δ_t in time, changing (6).

$$p_{phj}\left(t\right) = p_{ph}\left(t+\delta_t\right) - p_{ph}\left(t\right) \tag{7}$$

$$\approx \omega_0\delta_t P_{ph0}M\cos\omega_0 t = \delta_t\frac{d}{dt}p_{ph}\left(t\right) \tag{8}$$

The clock jitter noise added ($\delta\phi_t$) by the SC-circuit phases follows the same model.

Regarding the nonlinearity, we take the device transfer function at the operation point into account. Therefore (8) changes to:

$$p_{phjnl}\left(t\right) = d + c\left(e^{ap_{phj}} - 1\right) \tag{9}$$

Constants a, c and d were extracted from the physical properties of the emitter device.

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B. Noise source photodiode

The photodiode is the on-chip transducer in which, ideally, each incident photon with associated energy greater than or equal to the Si band gap would create an electron-hole pair (EHP). Throughout time, this EHP forms the photocurrent (I_{Ph}). We assume that the conversion photon to I_{Ph} does not dependent on time. Therefore, the two noise sources to be taken into account are the shot and the thermal ones [2]. The shot noise is caused by the dark current (I_{dark}) due to EHP generated in the space charge region and for the photocurrent I_{Ph}. Each of these currents is generated by independent random processes, and hence all contribute to the shot noise:

$$\overline{i_{sh}^2} = 2q\left(I_{Ph} + I_{dark}\right) \tag{10}$$

Thermal noise arises from the parasitic resistances (R_{in}) of the photodiode:

$$\overline{i_{th}^2} = \frac{4kT}{R_{in}} \tag{11}$$

Both currents should be evaluated in the bandwidth of interest.

C. Switch-Capacitor (SC) noise source

The switches have finite resistance, which supports internal random carrier fluctuations (thermal energy). Then, when ϕ_1 closes the switch and the V_{out} is "1", C_s integrates the signal with these fluctuations and the total noise is [3]:

$$\overline{e_{th}^2} = \int_{\infty}^{0} \frac{4kTR_{on}}{1+\left(\omega_0 R_{on} C_s\right)} df = \frac{kT}{C_s} \tag{12}$$

In fact, the amount of noise accepted due to $\overline{e_{th}^2}(t)$ is used to calculate the dimensions of C_s.

D. Integrator non-idealities

With the exception of the $\overline{e_{th}^2}$ noise, up to now the noise sources arise from optical, technological parameters and from inherent instrument noise. However, by choosing the circuits, we may obtain certain control over the non-idealities of the integrator.

The integrator design involves determining the b coefficient, the open-loop gain (A_{OL}), the range of diff-pair output voltage (v_{out}), unity gain bandwidth (UGBW) and the slew-rate (SR).

1) Finite DC gain effect: The SC-integrator z-domain transfer function from Fig. 1. The integrator ideal gain is $H(z) = bz^{-1}/(1-z^{-1})$, where $b = C_s/C_i$. For DC gain, $H(z)$ is infinite. In practice, however, the gain is limited by circuit constraints and by the diff-pair open-loop gain. The finite DC gain effect was modeled by integrator leakage: α, measures the output fraction, which is added to the new input sample to be integrated. Then:

$$H\left(z\right)|_{DC} = H\left(1\right) = b\frac{a}{1-\alpha} \approx A_{OL} \tag{13}$$

The result is that the $H\left(1\right)/b$ pole is displaced from the unit circle. This relation is also useful to estimate A_{OL}. Furthermore, the transfer function NTF is modified to:

$$NTF = \frac{\left(1-\alpha z^{-1}\right)}{1+\left(1-\alpha\right)z^{-1}} E\left(z\right) \tag{14}$$

If this new NTF is applied to (3) and (4) we may observe the SNR degradation; e. g. we take $A_{OL} = 48.8\,\mathrm{dB}$ and the simulation yields $SNDR = 58.7\,\mathrm{dB}$, which is just $1.1\,\mathrm{dB}$ less than the reference noise (SQNR). It is recommended that A_{OL} be greater than R, ensuring distortion for finite DC gain below $0.3\,\mathrm{dB}$ [1].

2) UGBW and SR effects: The integrator output voltage depends on the A_{OL}, and is determined by b coefficient and α leakage factor. In the C_i to C_s charge-transfer period $(nTs - Ts/2)$, the output voltage is $v_0\left(t\right) = \alpha V_0\left(1-e^{-t/\tau}\right)$, for $0 < t < \frac{T_s}{2}$.

The slope of this curve is the Slew-Rate, thus, the ideal value is when the maximum slope is reached.

$$SR_{max} = \frac{d}{dt}\, v_o\left(t\right)|_{t=0} = -\frac{\alpha V_o}{\tau} e^{\frac{-t}{\tau}}\Big|_{t=0} = \frac{\alpha V_o}{\tau} \tag{15}$$

If we consider that only one dominant pole exists, the step response is: $\tau = (1/2\pi)\, UGBW$, and thus the relationship between SR and UGBW: $SR_{max} = \alpha V_o 2\pi \cdot UGBW$.

The resulting model is shown in Fig. 3, which implements (8-15). We assumed that the noise is a Gaussian random process with standard deviations (or RMS noise value): δ_t, e_{th}, i_{th} and i_{sh} namely due to: jitter noise signal, SC-circuit noise, thermal and shot noise, respectively. Also SC-clock jitter is present with a standard deviation $\delta_{\phi t}$. The $UGBW$ and SR effects are gain integrator variations, as is placed before the integrator.

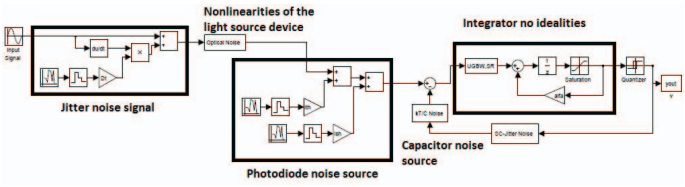

Fig. 3. Simulink modeling of different noise sources involved in the degradation of SQNR.

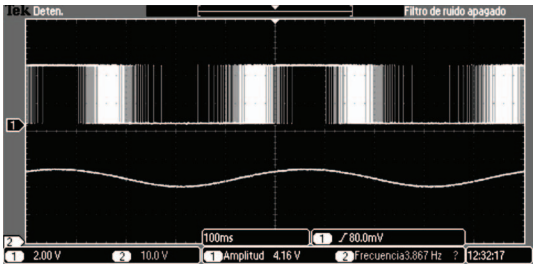

Fig. 4. Temporal response of first-order single-bit ΣΔM for sensing photocurrent

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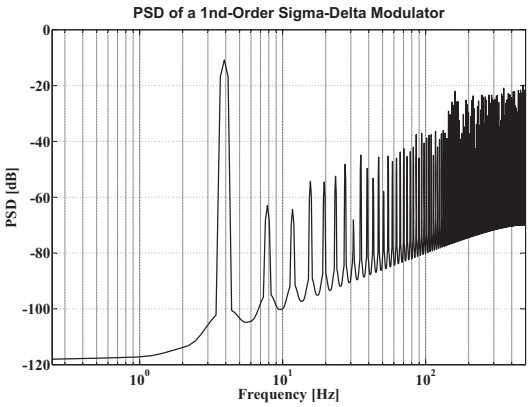

Fig. 5. PSD of ideal modeling

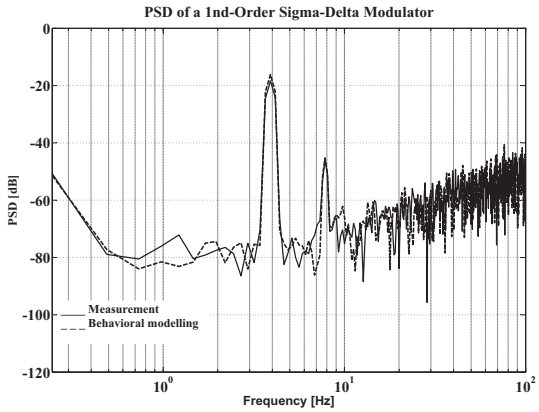

Fig. 6. PSD of real modeling

V. Results: Behavioral simulation Vs measurements

We made a spectral analysis of the excitation and clock phases to determine δ_t and $\delta_{\phi t}$. Since C_s is known, e_{th} was determined. Typical values for i_{sh} and i_{th} were taken into consideration. The values of these standard deviations are summarized in Table II.

The CIS prototype was mounted on a microscope to lead the modulated white light beam as indicated by (6). The light beam was applied only on the photodiode active area, and we took care to avoid background light noise. A time-domain result is shown in Fig. 4. The bottom signal is the excitation voltage of the light source and the top is the ΣΔM output signal. The density of 0's increased for low photocurrent ($\sim 50\,\mathrm{pA}$) and conversely the densities 1's increased for high photocurrent ($\sim 100\,\mathrm{nA}$). A selected test frequency that is within the bandwidth of the signal is $\sim 4\,\mathrm{Hz}$,

Fig. 5 shows the PSD obtained by the model including only quantization noise; there the NTF shapes the noise to high frequencies. In Fig. 6, the solid line shows the PSD of the measurement with $SNDR_T = 26.3\,\mathrm{dB}$, and the dashed line is the PSD by the proposed model with $SNDR_M = 28.3\,\mathrm{dB}$. These PSD show addition of DC components, due to a high noise floor and nonlinear components near of the bandwidth limit. The condition for this estimation and other ΣΔM specifications are presented in Table III.

TABLE II
RMS noise value and nonlinearities

δ_t	Jitter noise signal	$40\,\mu\mathrm{s}$
$\delta_{\phi t}$	SC-circuit jitter noise	$4\,\mu\mathrm{s}$
e_{th}	kT/C_s noise	$371.48\,\mu\mathrm{V_{RMS}}$
i_{th}	Thermal noise	$2\,\mathrm{nA_{RMS}}$
i_{sh}	Shot noise	$1\,\mathrm{nA_{RMS}}$
Constants of nonlinearities of the light source device $a = 0.2$, $d = -6 \times 10^{-3}$, $c = 0.81$		

TABLE III
ΣΔM ADC specifications

DR_{signal}	Dynamic range of the input signal	50 pA-100 nA
f_{Ny}	Nyquist's frequency	15.6 Hz
f_s	Sampling frequency	1 kHz
R	Oversampling rate	64
BW	Bandwidth of interest	7.81 Hz
N	Number of samples	4096
$SQNR$	Signal-to quantification-noise ratio	59.4 dB
$SNDR_M$	SNDR of the behavioral model	28.3 dB
$SNDR_T$	SNDR of the measurement	26.3 dB
THD	Total harmonic distortion	0.23 %

VI. Conclusion

It has been shown that a simple behavioral Simulink model predicts the temporal response of a first-order single-bit ΣΔM quite accurately, and determines the main noise sources that limit performance. On the other hand, the model may be useful for the extraction of electrical specifications of the integrator and the capacitors in the SC-circuits, thus improving circuit design. System level models were presented in [2] and [3] for second-order sigma modulators; however, the basic model presented here is intended to include optical parameters of the sensor (photodiode).

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