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Floating-Gate MOS Charge Programming Using Pulsed Hot-Electron Injection

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***Abstract*—The Floating-Gate MOSFET is a device which has many applications in the design of analog circuits. One drawback of its properties is the parasitic charge associated with its floating gate, usually present after the fabrication. Depending on the application, this charge needs to be removed or modified. This paper describes an algorithm and a prototype system which uses Fowler-Nordheim Tunneling and Hot-Electron Injection in a pulsed fashion in order to clear or modify the floating-gate charge.**

Keywords—FGMOS charge programming; floating gate; hot-electron injection; Fowler-Nordheim tunneling.

I. INTRODUCTION

The Floating-Gate MOSFET (FGMOS) is a device which has many applications in the design of analog circuits, although the design process is more complex given its increased degrees of flexibility. One obstacle in the generalized use of this device is the inability to precisely control the parasitic trapped charge that remains in the floating node after its fabrication. Such charge must be removed or modified before the device can be used. Many approaches have been devised for this task, but some require specialized equipment or complex circuitry embedded in the application circuit.

In this paper we present a method and a system that does not require the inclusion of complex circuitry in the design, nor calls for the use of special measurement equipment. It is specifically designed for the task of clearing the charge of a low number of FGMOS cells used in a Floating-Gate Delta-Sigma Modulator, although it can be used in many other scenarios, not only to clear but to modify the FGMOS charge as required. The paper is organized as follows. In section II we present the FGMOS device, its characteristics and usage and brief notes for its electrical simulation. Section III introduces the concepts of the physical phenomena used to modify the charge of the FGMOS. Section IV describes the generic algorithm proposed for the modification of the charge and section V briefly describes the system implementation. Finally, section VI gives a few results obtained from the use of our system.

II. THE FLOATING-GATE MOSFET

The FGMOS device is a standard MOS transistor, but its polysilicon gate is isolated by completely surrounding it by silicon dioxide, a high-quality insulator. A number of secondary gates or inputs are then deposited above the floating gate (FG). As there are no resistive connections to its gate, these inputs are only capacitively connected to the FG. The current of the transistor will be determined by the voltage of the FG, which is the result of the contributions of the voltages applied at the control inputs, the biasing of the transistor and any trapped charge present at the FG, as given by

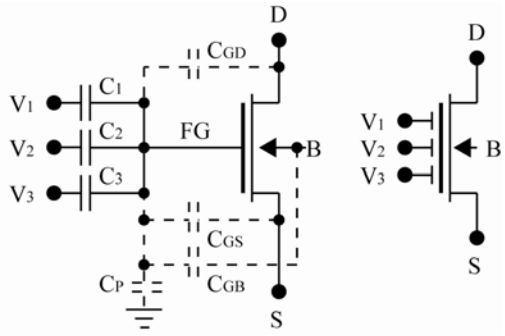

Fig. 1. Equivalent circuit and symbol for a three-input n-type FGMOS transistor.

$$V_{FG} = \sum_{i=1}^{N} \frac{C_i}{C_T} V_i + \frac{C_{GD}}{C_T} V_D + \frac{C_{GS}}{C_T} V_S + \frac{C_{GB}}{C_T} V_B + \frac{Q_{FG}}{C_T}, \quad (1)$$

where N is the number of inputs; C_i and V_i are the ith input capacitance and voltage, respectively; C_T is the total capacitance seen by the FG; and C_{GD}, C_{GS} and C_{GB} are the parasitic capacitive couplings between the FG and the drain, source and bulk, respectively. Q_{FG} is the positive charge trapped in the FG. The gate voltage can be substituted with (1) in any of the MOS transistor current laws, obtaining new expressions that are functions of the new input voltages. Fig. 1 shows the symbol and equivalent circuit for a 3-input p-type FGMOS transistor. Note that C_P represents the parasitic capacitance of the polysilicon FG to the substrate, i.e., outside of the active area. The ratio $k_i = C_i / C_T$ is the coupling factor for each input, and represents the weighted contribution each input voltage has over the FG voltage.

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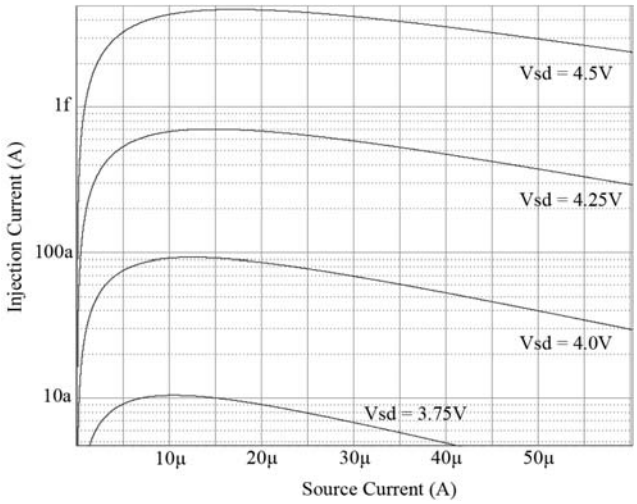

Fig. 2. HEI Injection efficiency – Injected Current versus Source Current. Each curve is shown for different Vsd values.

The electrical simulation of a FGMOS device presents challenges, since the FG is a floating node, without a DC path to ground. Although some simulation schemes have been proposed [1][2][3], we used a DC initial operating point and voltage ramping transient simulation methodology which does not require the use of complex models or circuits to emulate the behavior of the FG.[4]

The FGMOS offers a greater degree of freedom in the design of analog circuits, usually replacing a number of devices and thus reducing the complexity and power requirements. For example, it can be used as a voltage adder, a displaced threshold device, an analog memory or other circuits.

III. Floating-Gate Charge Modification

The design of analog circuitry with FGMOS makes compulsory to accurately control the amount of trapped charge present at the FG. The application will determine if it is necessary to modify such charge. In the case where the charge must be zero, a few schemes had been devised in order to get rid of the charge. One of the simplest approaches is the use of a fuse next to the FG.[5] Unfortunately, measurements have shown that this approach works only partially or not at all in some fabrication processes, leaving a residual charge that needs to be modified in either case.

The programming method proposed in this paper relies on two mechanisms for charge modification: the Fowler-Nordheim tunneling (FNT) and the hot-electron injection (HEI). The former will be used for the initial, coarse global "resetting" of all the FGMOS cells, while the latter will be used to provide the fine trimmed programming to the desired operating levels for each cell.

A. Fowler-Nordheim Tunneling

FNT is used to increase the positive charge (and hence the voltage) of the FG by removing electrons. A high voltage is applied at a tunneling junction, in this case, a shorted pMOS, increasing the electric field across the oxide and thereby

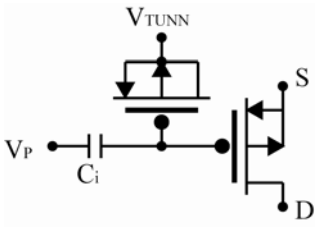

Fig. 3. Schematic of the FGMOS cell to be programmed. FNT will be performed on the shorted pFET, while the HEI is accomplished with the remaining transistor.

increasing the probability of the electron tunneling through the barrier. Due to the difficulty in isolating the FGMOS cells using high-voltage gates, FNT will only be used globally as a "reset".

B. Hot-Electron Injection

HEI is used to add electrons to the FG, decreasing the positive charge and therefore decreasing also the voltage. In order for injection to occur, two conditions need to be met, a high current flowing through the transistor's channel and a high gate-to-drain electric field. Channel holes, accelerated in the transistor's channel-to-drain depletion region, collide with the semiconductor lattice. When the channel-to-drain electric field is large, a fraction of these holes collide with sufficient energy to liberate additional electron-hole pairs. The ionized electrons, promoted to their conduction band by the collision, are expelled from the drain by this same channel-to-drain field. Electrons expelled with enough kinetic energy can, if scattered upward into the gate oxide, overcome the potential difference in electron affinities between the Si and SiO2, inject into the oxide conduction band, and be collected by the FG.[6]

C. HEI Efficiency

Although our system is devised for programming a low number of FGMOS cells, reduction of the programming time is desirable. Fig. 2 shows the injection efficiency curves for a typical transistor in the ON Semiconductor 0.5µm technology we used based on an empirical injection model [6] and whose parameters where found using a method described in [7]. The vertical axis is for the current injected in the FG through the oxide, and the horizontal axis is for the MOSFET Source current. The injection efficiency is defined as injected current over Source current. Each curve describes a different source-to-drain voltage. We observe that the peaks of efficiency are around 15µA, independent of the Vsd used.

IV. Programming Algorithm

The FGMOS cell that will be programmed in our application is shown in Fig. 3. Many FG charge programming approaches have been described in the literature.[8][9][10] The continuous programming scheme was considered[11] but later discarded due to the instability present with the current circuit configuration. Based on the need to program only a few cells, we chose to use a pulsed programming approach, where the cell is programmed based on a target output current, which can be determined by simulation of the FGMOS cell.

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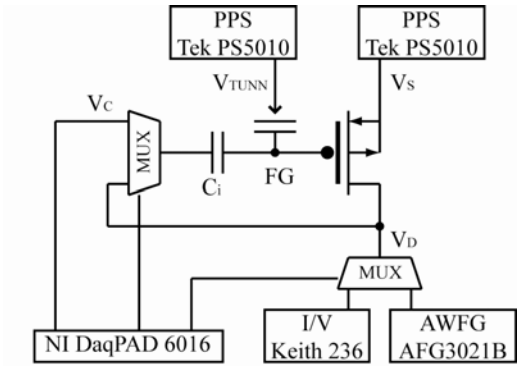

Fig. 5. Block diagram for the proposed Pulsed Current Injection System.

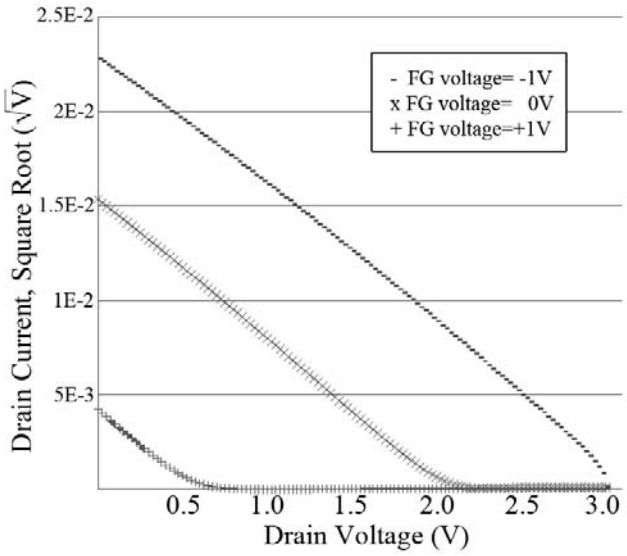

Fig. 4. I/V Curves for a diode-connected FGMOS device, showing the curve displacement obtained after programming with the proposed system, from zero-charge (middle trace) to 1V FG voltage and to -1V FG voltage. For the curve measurement, Vs = 3V.

A. *Algorithm*

As a first step, all cells are measured at their corresponding working voltages. For each cell, if the Drain current is below the intended target then the charge is above target too, and the cell can be programmed via HEI. If this condition is not met for every cell, a global reset tunneling pulse is applied for a long enough time to raise the charge of the FGs. This will allow using HEI to trim the target Drain current.

Next, for each cell the following steps are taken:

1. Raise the Source and Drain voltages to the injection levels, keeping at most a 3V of Vsd voltage to avoid electron injection in the FG. Then set the voltage at the V_P control terminal in such a way that the current during the HEI will approach the desired injection efficiency.
2. Apply a voltage pulse at the Drain for a specified time. The pulse is negative in order to reach the necessary source-to-drain voltage to cause electron injection. In this step the HEI is performed.
3. Revert the voltages at all terminals to the working voltages.
4. Measure the Drain current in working conditions. If the target Drain current has not been reached, repeat from step 1. If the target has been reached, then proceed with the next cell.

B. *Programming Voltages Choice*

The choice of the programming voltages, i.e., the Vsd and Vps, affects the injection efficiency and therefore the programming speed. As a first step, the approximate FG voltage can be determined by measuring the transistor Drain current under working voltage conditions. The equation for the FGMOS shown in Fig. 3 in the saturation region is

$$I_D = \frac{\beta}{2}\left(k_p V_{PS} + \left(k_{gs} - 1\right)V_S + V_Q - V_{TH}\right)^2 \qquad (2)$$

where k_p is the coupling coefficient for the control input, $k_{gs} = C_{gs}/C_T$ is the coupling coefficient for the source voltage by the C_{GS} parasitic capacitance and $V_Q = Q_{fg}/C_T$ is the effective voltage generated by the charge trapped in the FG. Solving for V_Q we readily see that

$$V_Q = -\sqrt{\frac{2I_D}{\beta}} - k_p V_{CS} - \left(k_{gs} - 1\right)V_S + V_{TH} \qquad (3)$$

Using this approximation and knowing the required Drain current for the peak injection efficiency at the injection biasing conditions, we can solve (2) for V_P, yielding

$$V_P = \frac{-\sqrt{\frac{2I_D}{\beta}} - \left(k_{gs} - 1\right)V_{Snj} - V_Q + V_{TH}}{k_p} + V_{Sinj} \qquad (4)$$

for an adequately selected source voltage V_{Sinj}, i.e., capable of generating the high-field required for the injection.

V. System Implementation

The physical implementation of the system was based on the available resources at hand. For the tunneling high-voltage and the source voltage, which were not required to switch quickly, a pair of Tektronix PS5010 programmable power sources where used. The current measurement was done with a Keithley 236 unit in a voltage-source/current-measure configuration. The programming pulses where produced from a Tektronix AFG3021B Arbitrary Waveform Generator, in order to provide fine pulse timing. Generic CMOS logic was used for the multiplexing of the signals. The biasing of the control input and the general mux control was provided by a National Instruments DaqPAD 6016 unit. The overall block diagram of the system is shown in Fig. 4.

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The algorithm programming and control execution was written in the National Instruments LabVIEW graphical environment. This tool provided good integration with the system hardware used. The graphical interface allowed the measurement and charting of the FGMOS V/I characteristics, tunneling timing and control and the basic algorithm execution. The interface is feed with the working and injection voltages, and target Drain current, and iterates until the target is reached. Manual control of the voltages is provided for real time modification of the injection conditions.

VI. TESTS

Fig. 5 shows the I/V curves of a diode-connected FGMOS device programmed with our pulsed injection system. The vertical axis units are square-rooted voltage, in order to show the diode characteristic and threshold voltage displacement obtained.

Programming times required using the programming voltages for maximum efficiency are very low, reaching and surpassing the target current in only two iterations for a half-second programming pulse. Obviously, for a fine-trimmed target current programming, various adjustments can be made:

- Reducing the Vsd voltage in order to reduce the injection efficiency and therefore the injection current.
- Reducing or increasing the Drain current by changing the voltage applied to the control input, in order to get away from the peak injection efficiency.
- Shrinking the programming voltage pulse duration.

A proposed approach is to calculate, for each iteration, the approximate FG equivalent voltage and the last measured Drain current delta, and calculate the best voltages to increase the efficiency and approach quickly the target Drain current. Then, detect when the measured Drain current is near the target Drain current and change to a regime of lower efficiency, in order to trim slowly and more precisely the required Drain current.

VII. CONCLUSIONS

A simple algorithm and a system requiring very little embedded extra circuitry and few equipment was presented. The concepts behind its operating principles were briefly explained. The built system was tested and found to have a good performance, and we suggested a few items to consider in order to improve the proposed system.

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