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# Floating Gate MOSFET Programming Circuit for Standard CMOS Technology

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*Abstract* —**In this work, we describe the low-complexity analog pulsed circuits for programming the electrical charge of floating gate p-channel transistors. These circuits control the injection current into the floating gate. The principle supporting the expected good resolution in this system comes from observing two operating cycles. In the first cycle, a constant injection current is applied then, in the second cycle, the resulting drain current is compared with a target current keeping the floating gate transistor inside the working analog circuit, where it belongs to. Both cycles, which are periodic and interleaved are valid until the target current is reached, event detected by a current comparator. This strategy seems to have no appreciable programming error. For the simulation results, it is introduced an injection current model supporting the technology used in this programming circuit namely, 0.5-micron, n-well, CMOS, whose electrical parameters were contained in the Mentor IC Nanometer Suite.**

*Keywords* —**FGMOS, pFGMOS, programming, CMOS, injection, hot electron injection, VLSI, floating gate, Mentor Graphics.**

## I. INTRODUCTION

At present, the p-channel, floating gate MOS transistor (pFGMOS) is taken as an essential element for analog memories and low frequency analog signal processing tasks [1,2]. The main drawback in the usage of the pFGMOS transistors is the need of removing and/or altering the electrical charge at the floating gate structure (an electrically isolated poly-silicon strip), which ultimately sets the threshold voltage parameter. Hot electron injection is a physical mechanism by which electrons generated by impact of holes in the channel near the drain gain energy enough to surpass the $SiO_2$ energy barrier injecting into the floating gate and therefore diminishing its total positive charge. By injecting electrons into the floating gate it is possible to diminish (program) its positive charge making the transistor a versatile device to use amidst a wide set of circuits. Usually 2 phases can be observed within the usage of pFGMOS transistors, one in which the programming is taking place and a second in which the pFGMOS is used within an application circuit. However, the resulting charge might change due to the effect of new voltages and equivalent capacitances when the programmed transistor is reconnected at the working circuit.

The programming protocol presented in [3] takes this problem into account and minimizes it for differential pairs in operational amplifiers. On the other hand, this approach is improved and applied to a large array of transistors in [4], increasing the programming resolution and velocity, but demanding a complex algorithm. In our work, observing the origin of the programming error as a charge redistribution feature, we propose a different programming system supported by external standard parts.

## II. PROGRAMMING PRINCIPLE

We show the programming principle in Figs.1 and 2, where M1, M2 and M3 are pFGMOS transistors sharing the same floating gate. During the programming cycle shown in Fig.1 the switch SW1 is opened, SW2 is closed and transistor M1 is used to inject electrons at a constant rate into this common floating gate, diminishing its total positive charge during a finite time T1 by applying voltages V1 and V2 to sustain a difference of Vsd ~ 5.1V. Transistor M2 is used as a bias transistor, fixing the potential Vg as a result of a constant current I_bias and also constant voltages V3 and V4. Both M1 and M2 are active during the programming cycle (Fig.1) and passive during the analog cycle (Fig.2). The programming and the analog cycles appear in two time intervals T1 and T2 respectively. Also T1+T2 conform the period T, whose frequency is F = 1/T. In both Figs. 1 and 2, V1 through V6 along with VDD1 and VDD2 are DC levels.

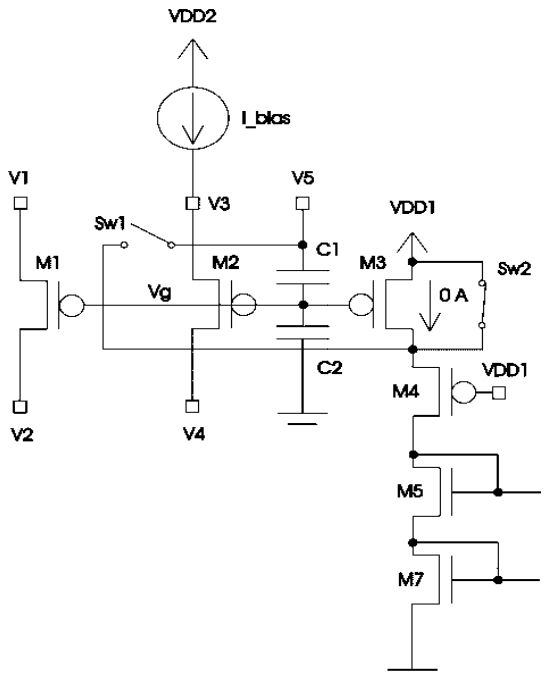


**Fig. 1** Circuit representing the programming cycle.

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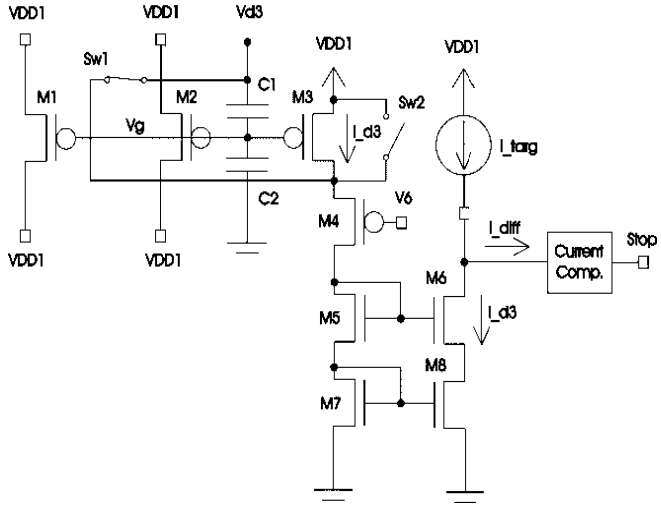


**Fig. 2** Circuit representing the analog cycle.

During the analog cycle (T2) we make transistors M1 and M2 passive by applying voltage VDD1 to its source and drain terminals and M3 active by closing switch SW1 and opening switch SW2 as can be seen in Fig.2. Due to the programming cycle and the activation of transistor M3 the voltage in the floating gate changes resulting from the charge redistribution ΔQ into C1, C2, Cox1, Cox2; where Cox1 and Cox2 are the gate capacitances of M1 and M2, respectively. ΔQ is the electronic charge injected in a single programming cycle.

Voltages V3 and V5 come from a gain block with feedback and their values are observed as: 1) V3 follows an external DC voltage and, 2) the change of V5 namely, ΔV5 obeys to the capacitive balance: ΔV5=Q/C1 (other parasitic capacitances are neglected); where Q is the present injected charge, C1 is defined by geometrical layout and C2 is the parasitic capacitance resulting of the bottom plate of C1. The injection current of electrons into the floating gate can be estimated using the model below.

$$I\_inj = \alpha I_S exp\left(-\frac{\beta}{(\mathrm{Vg}-\mathrm{V2}+\delta)^2}+\lambda\,(\mathrm{V1}-\mathrm{V2})\right)$$

Where Is is the source current of M1. This model was originally reported for 0.35-micron CMOS technology in [5], with: $\alpha = 1.30\text{x}10^{-5}$, $\beta = 155.75$, $\delta = 0.702$, $\lambda = 1.0$; on the other hand, the same parameters (α, β, δ and λ) for the 0.5-micron, n-well, CMOS technology have been recently computed in a parallel work [6], following the Levenberg-Marquardt optimization method from experimental data on fabricated floating gate transistors, getting:

$\alpha = 70\text{x}10^{-5}$
$\beta = 1415$
$\delta = 4.683$
$\lambda = 1.695$

The analog current I_d3 is periodically copied by the cascode array (formed by transistors M5, M6, M7 and M8), whose output is subtracted from a reference current (or target current, I_targ). The sign of the difference current I_diff, which is given by a current comparator block, determines stopping the programming process. Thus, when I_d3 equals I_targ, the whole of injected charge is given as: Qtotal=(N)(T1)(I_inj), where N is the count of pulses used to reach I_targ. Likewise, the change of Vg is given by (1):

$$\Delta V_g = \frac{Q_{total}}{C_{ox1}+C_{ox2}+C_1+C_2} \quad \textbf{(1)}$$

## III. SUPPORTING ANALOG AND DIGITAL COMPONENTS

This section presents the entire programming circuit that includes analog and switching components, which are some integrated and other external. In Fig. 3 is the electrical diagram of the actual programming circuit is shown. Integrated transistors Ms1, Ms2, Ms3, Ms4 and Ms5, act as the switches SW1 and SW2 shown in Fig.1 and Fig.2 to change the circuit between the functionality of the programming cycle and the analog cycle. The external parts are the gain blocks: OpAmp1 (along with OpAmp2 and OpAmp3, not shown in Fig. 3); OpAmp2 and OpAmp3 belong to the current sources I_bias and I_targ, whose electrical diagrams are shown in Figs. 4 and 5. Both current sources use an integrated p-channel transistor (M9 and M10) with an external resistor (R1 and R2). OpAmp1, OpAmp2 and OpAmp3 are LMC662 electronic parts, with 0V-12V DC supply. R1 and R2 are $10\text{x}10^6$ ohm each; V7 and V8 are DC voltages for regulating a 100 nA-current. The capacitor C1 is 0.1 pF (thus, C2 is 0.017 pF). Table I presents the states of the pulsed voltages: V_pulse1 through V_pulse6 at T1 and T2. In fact, these pulsed voltages should be generated by standard electronics; they are not shown in this work. Lastly, the current comparator block might be integrated based on contemporary designs; one candidate is in [7].

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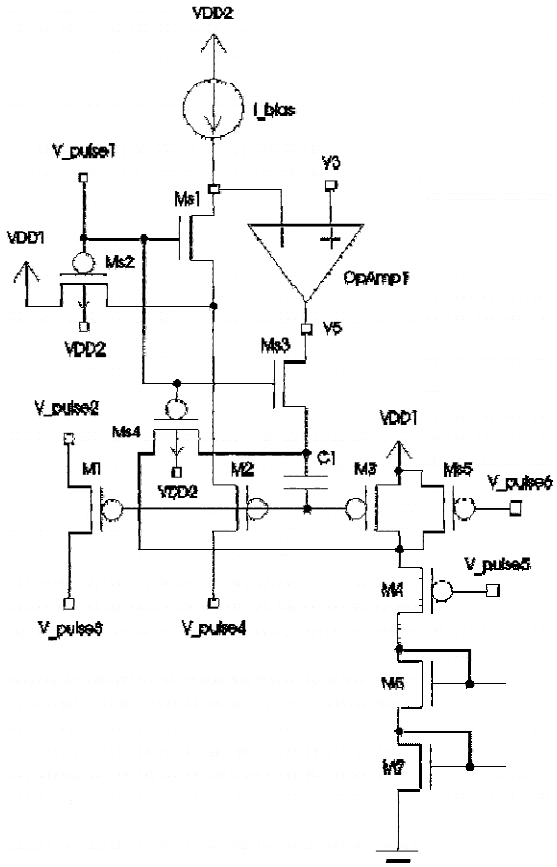


**Fig. 3** Detailed programming circuit.

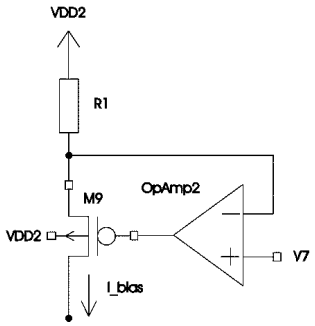


**Fig. 4** Implementation of I_bias current source.

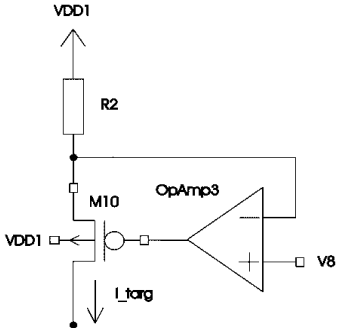


**Fig. 5** Implementation of I_targ current source.

**Table I**

| Cycle =>> | "Programming" (T1) | "Analog" (T2) |
|---|---|---|
| V_pulse1 | VDD2 | GND |
| V_pulse2 | V1 | VDD1 |
| V_pulse3 | V2 | VDD1 |
| V_pulse4 | V4 | VDD1 |
| V_pulse5 | VDD1 | V6 |
| V_pulse6 | GND | VDD1 |

## IV. ELECTRICAL SIMULATION

This programming circuit was simulated using 0.5-micron, n-well, CMOS ON Semiconductor electrical parameters. The initial floating gate voltage (Vg) is established ramping from ground to the working voltage all DC voltage sources. This procedure, which avoids lack of convergence in DC [1], considers the ideal case where Q=0. Table II shows the size ratio, W/L in micro/micron for all analog transistors, and Table III does for the switching transistors. The DC voltage levels for supply and switching pulses are in Table IV. Figs. 6 and 7 show two snapshots of 10 ms each at the beginning and at the end of the programming process, respectively for the injection current in M1 (Figs. 6a and 7a), and for the floating gate voltage Vg (Figs. 6b and 7b). For this sample simulation, a frequency of 1 KHz in the switching pulses with T1= 0.5 ms and T2=0.5 ms is considered. Also, the analysis is done in the time interval [0 s, 10 s]. During the "programming" cycle, where Ibias is 100 nA, M2 sets Vg at 3.723 V, (its source-drain voltage is kept at 2.0 V); transistor M1 provides a constant injection current value of 15.82 fA, meanwhile its source current is 1.97 uA. The programmed transistor M3 experiments a change of its drain current from 0.745 nA (at time 0.005 s) to 1650 nA (at time 10 s), which is associated to the change of the floating gate voltage: 309 mV (from 2.378 V to 2.069 V).

**Table II**

| | |
|---|---|
| M1 | 0.6/0.9 |
| M2 | 0.6/9.0 |
| M3 | 0.6/9.0 |
| M4 | 0.6/9.0 |
| M5 | 7.5/7.5 |
| M6 | 7.5/7.5 |
| M7 | 7.5/30.0 |
| M8 | 7.5/30.0 |
| M9 | 9.0/0.6 |
| M10 | 9.0/0.6 |

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**Table III**

| | |
|---|---|
| Ms1 | 0.9/0.6 |
| Ms2 | 0.9/0.6 |
| Ms3 | 0.9/0.6 |
| Ms4 | 0.9/0.6 |
| Ms5 | 0.9/0.6 |

**Table IV**

| | |
|---|---|
| VDD1 | 3.0 V |
| VDD2 | 6.5 V |
| V1 | 5.1 V |
| V2 | 0 V |
| V3 | 4.5 V |
| V4 | 2.5 V |
| V5 | 4.42 V |
| V6 | 2.0 V |
| V7 | 5.5 V |
| V8 | 2.0 V |

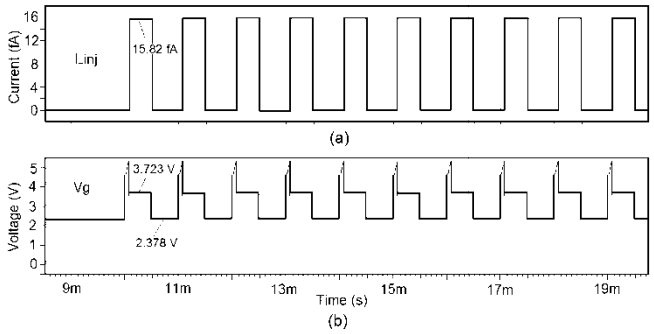


**Fig. 6** (a) constant injection current (b) floating-gate voltage at the first 10 pulses.

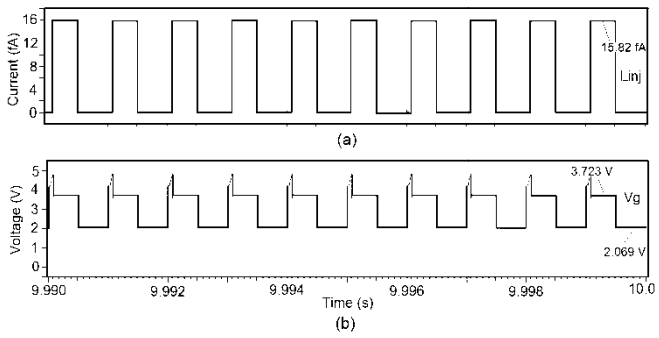


**Fig. 7** (a) Constant injection current (b) floating-gate voltage at the last 10 pulses.

## V. CONCLUSION

An analog pulsed programming principle is presented in this work to inject a constant finite current of electrons into the floating gate of pFGMOS transistors during each programming pulse until a target drain current is reached. We used an injection current model fit describing the standard CMOS 0.5-micron, n-well, technology. There is a wide interval of drain current values (3 orders of magnitude, from nA to uA) in which the programming target current can be reached using a representative analog transistor. Also, the time for programming is in the order of tens of seconds. It remains estimating the accuracy of programmed current as a function of the time in the "programming cycle" namely, T1. This technique might be suitable for treating a low number of floating-gate transistors inside an analog prototype and reducing the need to instrumental systems.

## REFERENCES

[1] Low Power and Low Voltage Circuit Design with the FGMOS Transistor. Rodriguez-Villegas, E. IET Circuits, Devices and Systems Series 20 (2006, The Institution of Engineering and Technology, London, UK).

[2] Learning on Silicon. Adaptive VLSI Neural Systems. Cauwenberghs, G. and Bayoumi, M.A. (Eds.). Kluwer Academic Publishers (1999).

[3] A Precision CMOS Amplifier Using Floating-Gate Transistors for Offset Cancellation. Srinivasan, V., Serrano, G.J., Gray, J. and, Hasler, P. IEEE J. Solid-State Circuits, Vol. 24, No. 2, (2007), pp. 280-291.

[4] Adaptive Algorithm Using Hot-Electron Injection for Programming Analog Computational Memory Elements within 0.2% Accuracy Over 3.5 Decades. Bandyopadhyay, A., Serrano, G.J., and Hasler, P. IEEE J. Solid-State Circuits, Vol. 41, No. 9, (2006), pp. 2107-2114.

[5] A Simulation Model for Floating-Gate MOS Synapse Transistors. Rahimi, K., Diorio, C., Hernandez, C., and Brockhausen, M.D. 2002 International Symposium on Circuits and Systems, ISCAS 2002, Vol. 2, pp. II-532 - II-535.

[6] Injection Current Model Fitting in p-Channel Floating-Gate MOS Transistors Using the Levenberg-Marquardt Method. Hernandez-Garnica, O., Gomez-Castañeda, F., Moreno-Cadenas, J.A., and Flores-Nava, L.M. 2013 International Conference on Electrical Engineering, Computing Science, and Automatic Control, CCE 2013, Sept. 2013, Mexico City, Mexico (to be published in this proceedings series).

[7] Low-Power High-Speed Current Comparator Design. Banks, D., and Toumazou, C. Electronics Letters, Vol. 44, No. 3, (2008), pp. 171-172.

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ISBN 978-1-4799-1461-6