

CCE

CCE 2020

2020, 17th International Conference on Electrical Engineering, Computing Science and Automatic Control

**Mexico City, Mexico.
November 11-13, 2020**

CALL FOR PAPERS

The main goal of CCE is to provide a forum for free discussion and interchange of research and development experiences and ideas, in the fields of electrical-electronics engineering, computer science and automatic control.

This conference also offers an opportunity for younger researchers and students to meet more experienced colleagues from different parts of the world. Conference content will be submitted for inclusion into IEEE Xplore as well as other Abstracting and Indexing (A&I) databases.

Submitted manuscripts should be six (6) pages or four (4) pages in IEEE two-column format, including figures, tables, and references.

General Chairs

Dr. Gerardo Silva Navarro
Dr. Wen Yu Liu
Dr. Sergio Salazar Cruz

Information

Address: Av. Instituto Politécnico Nacional
2508, Col San Pedro Zacatenco,
Alcaldía Gustavo A. Madero
City: Mexico City
Country: Mexico
CP: 07360
Phone: +52 (55) 5747-3800 Ext 6503
FAX: +52 (55) 5747-3976
cce@cinvestav.mx

Deadline

Full Manuscript: **July 6, 2020** extended to **August 14, 2020**
Review Notification (Phase 1): **Before September 4, 2020**
Final Revised Manuscript: **September 18, 2020**
Verification of final manuscript and
Papers accepted (Phase 2): **September 28, 2020**
Submit Payment (Authors): **October 12, 2020**

Topics

Include but not limited to:

- Automatic Control
- Computer science and computer engineering
- Biomedical engineering
- Communications systems
- Mechatronics
- Mechanical Engineering
- Aeronautic and Aerospace Engineering
- Solid-state materials, electron devices and integrated circuits
- Power Electronics
- Nanotechnology (materials and applications)
- Autonomous Navigation
- Exoskeletons

In support of the health contingency due to COVID19, registration costs has been reduced



<http://cce.cinvestav.mx>

ISSN
Online: 2642-3766

ISBN
978-1-7281-8987-1



Cinvestav

Design of position sensor of a linear micromotor based on CMOS-MEMS technology

Andrea López-Tapia
 Electrical Engineering Dept.
 CINVESTAV-IPN
 Mexico City, Mexico
 andrea.lopez@cinvestav.mx

Mario Alfredo Reyes-Barranca
 Electrical Engineering Dept.
 CINVESTAV-IPN
 Mexico City, Mexico
 mreyes@cinvestav.mx

Griselda Stephany Abarca-Jiménez
 UNIDAD PROFESIONAL
 INTERDISCIPLINARIA
 CAMPUS HIDALGO
 INSTITUTO POLITÉCNICO
 NACIONAL
 Hidalgo, 42162, Mexico
 Mexico City, Mexico
 gabarcaj@ipn.mx

Luis Sánchez-Márquez
 Electrical Engineering Dept.
 CINVESTAV-IPN
 Mexico City, Mexico
 luis.sanchez.m@cinvestav.mx

Luis Martín Flores-Nava
 Electrical Engineering Dept.
 CINVESTAV-IPN
 Mexico City, Mexico
 lmflores@cinvestav.mx

Abstract— This paper shows the design of the position sensor, consisting on a structure composed by a structural aluminum layer whose purpose is to act as a linear electrostatic micromotor; it has also a polysilicon layer acting as part of the proposed position sensor, which will operate as a floating gate of a MOS transistor (FGMOS). This structure is designed under the rules of the standard 0.5 micron CMOS technology. Through this, a relation between the position of the micromotor and the current through the FGMOS is obtained. The simulations were obtained using PSpice.

Keywords—MEMS, Linear Electrostatic Micromotor, Position Sensor, FGMOS

I. INTRODUCTION

Floating gate MOS transistor (FGMOS) technology is a mature technology, which had its beginnings in the 1960s, when Kahng and Sze reported the first floating gate structure [1]. They established as the main characteristic of the FGMOS, the ability to induce electric charge in the floating gate without physical contact and maintaining it for large periods of time.

Floating gate transistors have been widely used in different applications to store digital information, in structures such as EPROMs, EEPROMs, and flash memories [2], as well as a transducer element in capacitive sensors such as accelerometers [3] or in inertial sensing MEMS devices with 0.5 micron CMOS technology [4].

With this background, it can be said that there are very few designs compatible with the standard CMOS technology, which contain the mechanical structure of the micromotor, the control circuit and the position sensor in the same chip. This implies that its cost is lower. The position sensor that was developed in the present work is an element of the linear micromotor [5] shown in Fig. 1, which has a stepping motion.

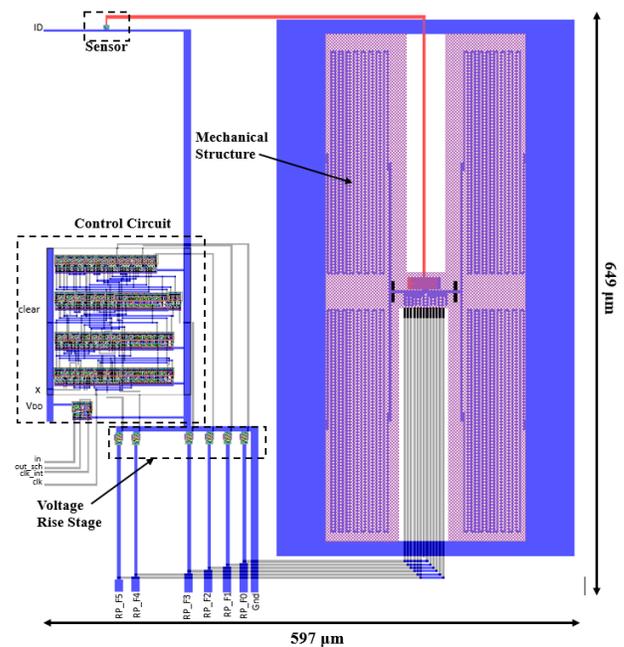


Fig. 1. Topological design of the linear micromotor system.

II. FLOATING GATE MOS TRANSISTOR (FGMOS)

One of the elements included in the design explained in this work is the floating gate MOS transistor (FGMOS). The proposed approach for this device is to function as a position sensor of a micromotor, and it is an innovation that is included

in the development of this type of system and it should be considered as a CMOS-MEMS approach since the micromotor will be designed as a micro-electro-mechanical-system (MEMS).

The FGMOS (Floating Gate MOSFET) is a field effect transistor, whose structure is similar to the conventional MOSFET, however it has a gate that is electrically isolated, creating a floating node as well as one or more control gates. The structure is shown in Fig.2. The floating gate, made of polycrystalline silicon, is separated from the transistor channel region by a thin oxide and from the control gate by a thick oxide.

The capacitive equivalent circuit for the FGMOS is shown in Fig. 3. Where C_G is the capacitor formed by the control gate and the floating gate, C_D is the capacitor formed by the overlap between the drain and the floating gate, C_S is the capacitor formed by the overlap between source and floating gate, C_{ox} is the capacitor formed between substrate and floating gate within the active area, C_{poly} is the capacitor formed between substrate and floating gate outside the active area. V_{CG} , V_D , V_S and V_B are the voltage applied to the control gate, drain, source and bulk, respectively.

The floating gate potential (V_{FG}) is determined in function of the capacitive coupling of the floating gate with the control gate, and in an undesirable way with other parasitic potentials coupled to the floating gate, this relationship is shown in (1).

$$V_{FG} = K_{CG}V_{CG} + \frac{C_D}{C_{TOT}}V_D + \frac{C_S}{C_{TOT}}V_S + \frac{C_{OX}}{C_{TOT}}V_B + \frac{Q_{FG}}{C_{TOT}} \quad (1)$$

Where $K_{CG} = C_G/C_{TOT}$ is the coupling coefficient and $C_{TOT} = C_G + C_D + C_S + C_{OX} + C_{Poly}$ is the total capacitance that represents all the existing capacitances. Q_{FG} is the residual charge stored in the floating gate (the one that is trapped in the material during the manufacturing process and whose magnitude and polarity is random).

The current I_D (as shown in Fig. 4) in the saturation region is dependent on the value of the coupling coefficient, therefore it depends on the value of the capacitances, especially of the capacitor formed by the control gate and the floating gate, since compared to other parasitic capacitances, it is more significant. Therefore, from (1) it can be seen that if the coupling coefficient (K_{CG}), is variable, the current of the FGMOS, given by (2), will also vary as a function of K_{CG} . This was used to design the position sensor circuit.

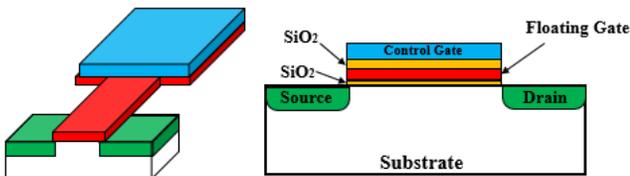


Fig. 2. FGMOS structure and cross section.

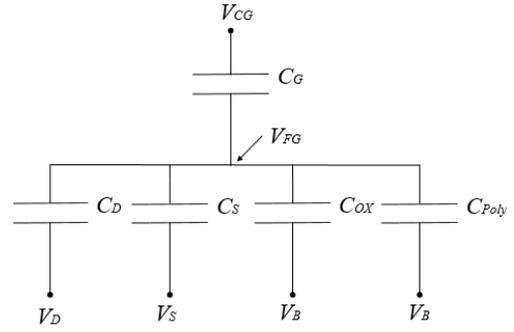


Fig. 3. Capacitive equivalent model.

$$I_D = \frac{\beta}{2}(V_{FG} - V_{TH})^2 = \frac{\beta}{2} \left(\frac{C_G}{C_{TOT}} V_{CG} - V_{TH} \right)^2 \quad (2)$$

Where β is the transconductance parameter and $V_{TH} = 0.6V$ is the threshold voltage for an N channel MOSFET.

A. Floating gate discharge techniques

Since in the design explained in this work, it is required to operate with the floating gate discharged, it is necessary to use one of the following discharge techniques [6] to eliminate the residual charge stored in the floating gate (Q_{FG}):

- Discharge of the floating gate through illumination with ultraviolet light (UV). It consists in applying a flow of ultraviolet light over the floating gate, inducing the temporary generation of conductances (stimulated by UV light) between drain-floating gate and source-floating gate, through which the discharge of the floating gate can be achieved.

- Discharge of the floating gate by Fowler-Nordheim tunneling (FN). It consists in applying a high voltage to the control gate (G) which produces a Fowler-Nordheim tunneling (due to the presence of a high electric field in G). Depending on the polarity of the voltage, the charge is transferred from the control gate to the floating gate or from the floating gate to the control gate. The amount of charge transferred from one gate to the other is a function of the time the high voltage is applied and its magnitude.

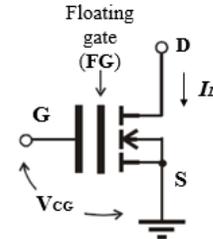


Fig. 4. Transistor FGMOS symbol.

- Floating gate discharge by temporary connection to substrate, during the manufacturing process. In this method, a contact is made from the floating gate to the last metal layer available in the manufacturing process (in this case Metal3 in the On Semiconductor 0.5 micron CMOS process). On the other hand, a contact is made from the substrate to this metal layer. During the manufacturing process, when the Metal3 layer is completely deposited, there is a temporary contact between the floating gate and the substrate, keeping it discharged through it. Finally, when the attack on the Metal3 layer is made, the floating gate ends completely discharged.

III. DESIGN OF THE POSITION SENSOR

In order to add particular characteristics to the design of the micromotor prototype, the use of the FGMOS transistor is proposed here to correlate the position of the mobile electrodes with the current delivered by the transistor, so that the change in the coupling coefficient can be used by adding a movable plate as a control gate. This is accomplished by varying the overlap with the floating gate. Thus, the position sensor is made with an FGMOS as a transducer element, this is, it will give different I_D values for each position. This sensor is made up of a control gate, a floating gate, drain and source, as explained above.

Due to the type of movement that the motor performs [5], there should be no obstacles in its path. It is chosen to place the control gate attached to the moving part in the same layer (Metal 1-Aluminum in order to have greater rigidity of the mobile mechanical structure because of its thickness of $0.64\mu\text{m}$) where the electrodes are as shown in Fig. 5. It can be seen in the same figure, the floating gate just below the control gate (Poly 1). In this way, they will have no friction between them after the surface micromachining and the MOS transistor remains fixed with the floating gate.

When the mechanical structure made with the Metal 1 layer is displaced by applying an electrostatic force due to the interaction between the electrodes of the linear micromotor [7], the area of overlap between the control gate and the floating gate varies (as shown in Fig. 6). Consequently, also the C_G capacitance that was discussed in section II varies, producing a change in the drain current (I_D).

Since the variation of drain current (I_D) depends on the overlap area, it is important that there is always an overlap area regardless of the position of the motor; otherwise, there would be positions with meaningless I_D values.

For this proposal, it is important to take into consideration the micromachining (that is, etching the silicon oxide, sacrificial layer) of the mobile electrodes area, as well as the region where the control gate is attached to them. This should be considered when making the topological design to leave appropriate indications, following known strategies, so that this region is ready to be able to do the surface micromachining and release the mobile mass and the control gate. However, it must be taken special attention that this window, included to allow micromachining, does not include the FGMOS gate oxide region, this is, the channel region.

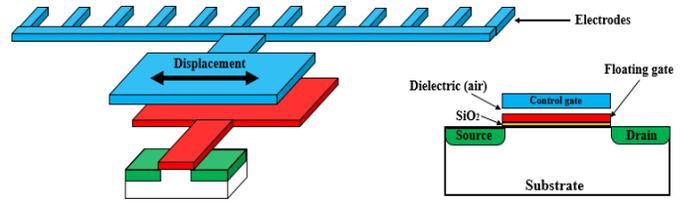


Fig. 5. Sensor structure.

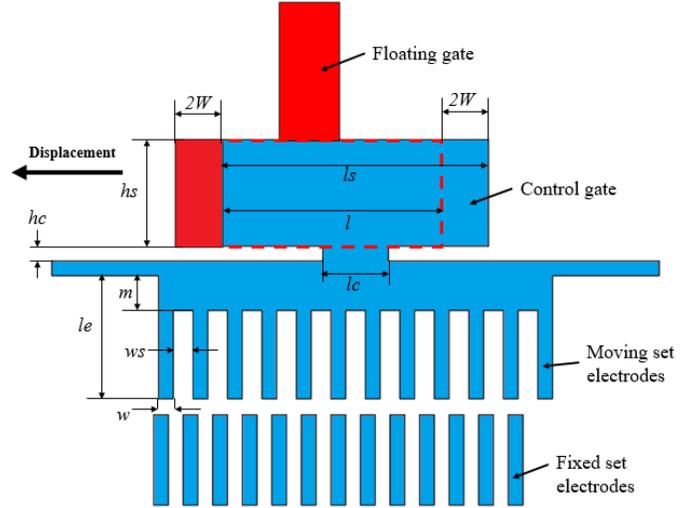


Fig. 6. Overlapping sensor top view.

A. FGMOS and electrodes dimensions

To give dimensions to the control gate, it is necessary to take into account the following aspects: the size of the electrodes and that the structure is only attached to two pair of springs as shown in Fig. 7, since the structure could have a slight torsion. Therefore, it is very important to keep it in static equilibrium, this is, both sides must weigh the same, both the control gate and the moving set electrodes. Hence, this will be a design criterion to be followed for the design of the mobile structure. Once this is accomplished, the total displacement of the motor must also be considered, in this case after six steps (2 times the width of the electrodes, this is, $2W$) forwards and backwards as shown in Fig. 6.

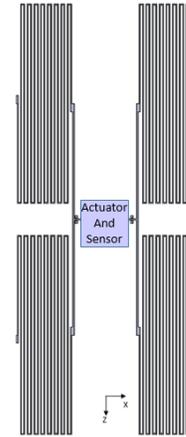


Fig. 7. Mechanical structure of the micromotor.

The way to ensure the same weight on both sides is to equalize the sensor (Control gate) and electrodes areas as shown in (3).

$$A_{sensor} = A_{electrodes} \quad (3)$$

Based on the dimensions shown in Fig. 6, the above equation is expressed as follows in (4):

$$hs \cdot ls + hc \cdot lc = 12(le \cdot w) + 11(m \cdot ws) \quad (4)$$

All values except m are proposed; thereby it results with a value of $4.23 \mu\text{m}$. In the initial position before starting the motor movement, the control gate and the floating gate have an overlap of $28.8 \mu\text{m}$ as shown in Fig. 8, and both control gate and floating gate have the same size.

B. Capacitance variations

As already explained above, a variation in the drain current (I_D) is obtained for each step taken by the motor, because the overlap area varies and in the same way C_G (the capacitor formed by the control gate and the floating gate). It is necessary to calculate C_G in each step with (5) to obtain I_D .

$$C_G = \frac{l}{k_0} [CMIP \cdot l \cdot hs + CMIPP(2l + 2hs)] \quad (5)$$

Where k_0 is the dielectric constant of silicon oxide. The equation is divided by this constant, because in the case of this capacitance the dielectric is air, $CMIP$ is the capacitance per unit area between the Metal 1 and Poly1 layer, $CMIPP$ is the capacitance per unit length between the Metal 1 and Poly 1 layer, both constants can be found in the MOSIS wafer electrical tests [8], hs and l are the dimensions of the overlapping area at each step. Table I shows the value of all the constants used, which correspond to the technological parameters provided by the 0.5 microns MOS technology of On Semiconductor.

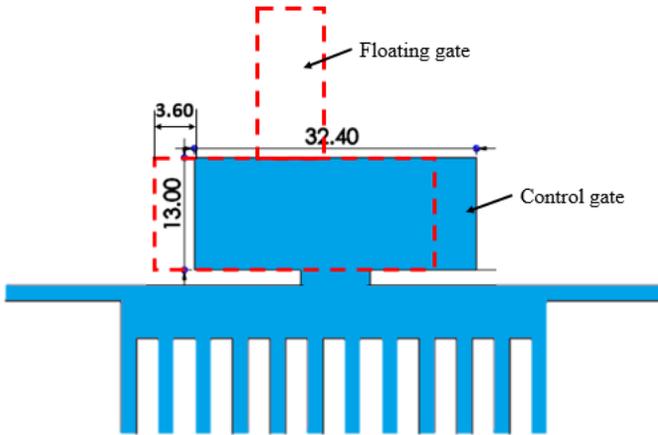


Fig. 8. Sensor dimensions (μm).

TABLE I. PARAMETERS FOR C_G CALCULATION

Parameter	Value
Dielectric constant of SiO_2 (k_0)	3.97
Capacitance per unit area Metall-Poly1 layer ($CMIP$)	61 fF/ μm^2
Capacitance per unit length Metall-Poly1 layer ($CMIPP$)	67 fF/ μm
Width of the overlapping (hs)	13 μm

Table II shows the value that C_G takes in each step, calculated with (5), taking into consideration the dimensions obtained and the values given in Table I. In each step the overlap changes, this is, dimension l is changing.

As already explained in section II the coupling coefficient can be obtained by $K_{CG} = C_G / C_{TOT}$, however the value of the total capacitance C_{TOT} given by (6) must be calculated.

$$C_{TOT} = C_G + C_D + C_S + C_{OX} + C_{Poly} \quad (6)$$

All the necessary parameters to obtain all the previous capacitances are in Table III

TABLE II. C_G VARIATION

Position	l (μm)	C_G (fF)
Initial (Step 0)	32.4-3.6=28.8	7.164
Step 1	28.8+0.6=29.4	7.304
Step 2	28.8+2(0.6)=30	7.444
Step 3	28.8+3(0.6)=30.6	7.584
Step 4	28.8+4(0.6)=31.2	7.724
Step 5	28.8+5(0.6)=31.8	7.864
Step 6	28.8+6(0.6)=32.4	8.004

TABLE III. PARAMETERS FOR CAPACITANCES CALCULATION

Parameter	Value
Electrical Permittivity ($\epsilon_{ox} = k_0 \epsilon$)	$3.513 \cdot 10^{-11} \text{ C}^2/\text{Nm}^2$
Width of FG MOS channel (Wc)	2.4 μm
Length of FG MOS channel (Lc)	0.9 μm
Oxide thickness (T_{ox})	$1.41 \cdot 10^{-8} \text{ m}$
$CGBO$ [9]	$1 \cdot 10^{-9} \text{ F/m}$
LD [9]	$7.469087 \cdot 10^{-8} \text{ m}$
WD [9]	$2.526685 \cdot 10^{-7} \text{ m}$
Capacitance Poly1-substrate (CPS) [9]	$8.8 \cdot 10^{-17} \text{ F}/\mu\text{m}^2$
Floating gate area out of FG MOS active zone ($A_{CG} = ls \cdot hs$)	421.2 μm^2

The parasitic capacitance value between drain and floating gate (C_D) is given by (7) [10].

$$C_D = \frac{\epsilon_{ox}LD(W_C - 2WD)}{T_{ox}} = 3.526259 \cdot 10^{-16} F \quad (7)$$

The value of the parasitic capacitance between source and floating gate is given by $C_S = C_D = 3.526259 \cdot 10^{-16} F$. The value of the parasitic capacitance between substrate and floating gate (C_{OX}) within the FGMOS active area is given by (8).

$$C_{OX} = CGBO(Lc - 2LD) = 7.506183 \cdot 10^{-16} F \quad (8)$$

The parasitic capacitance value between substrate and floating gate outside the FGMOS active area is given by (9).

$$C_{Poly} = A_{CG} \cdot CPS = 3.707 \cdot 10^{-14} F \quad (9)$$

Finally, it can be seen that the total capacitance practically depends only on C_G and C_{Poly} , because the other capacitances are almost negligible compared to these two. Therefore, if C_G has an ascending behavior, the same behavior will have the value of the coupling coefficient at each position. Fig. 9 shows how the K_{CG} varies for each position when the motor is moving forward and backward.

Since a voltage of 16 V (V_{motor}) as shown in Fig.10 will be present in the control gate, it is important to consider that when working with CMOS devices with 0.5 μ m technology, there is a thickness $t_{ox} = 14.1$ nm and it can have a maximum electric field of $\epsilon_{MAX} = 7$ MV/cm. Therefore a maximum voltage can be applied to the floating gate of $V_{MAX} = \epsilon_{MAX} t_{ox} = 9.87$ V. It is important to consider this value within the design of the FGMOS, in this manner this voltage is not exceeded to take care of the physical integrity of the transistor. However due to the presence of the floating gate, the actual voltage applied at the CMOS gate is the floating gate voltage (V_{FG}).

The floating gate voltage is given by (1), however to make an approximation only the first term is considered, since the other capacitances are negligible and the charge on the floating gate is zero, therefore the equation used is (10).

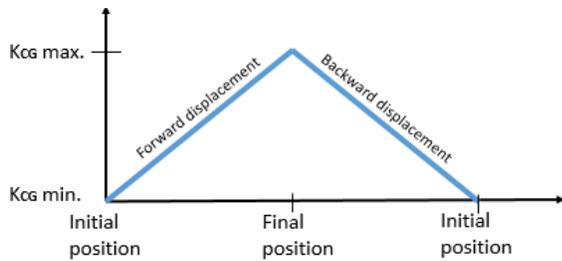


Fig. 9. K_{CG} behavior.

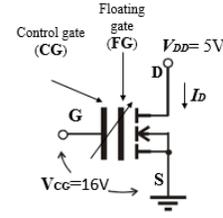


Fig. 10. Applied voltages in FGMOS.

$$V_{FG} = K_{CG} V_{CG} \quad (10)$$

If we substitute the value of the maximum coupling coefficient $K_{CG \text{ Máx}} = C_{G \text{ Máx}} / C_{TOT} = 8.004 \text{fF} / 49.5 \text{fF} = 0.16$ and a voltage between control gate and source of $V_{CG} = 16$ V, a value of $V_{FG} = 2.56$ V is obtained, which does not exceed the maximum value allowed of 9.87V for a MOS transistor.

IV. RESULTS

In this section, the electrical operation of the FGMOS is evaluated in the voltage range within which the associated electronic circuit will be operating.

To perform the simulation, the PSpice program is used, in which it is made a list with the voltages applied to the FGMOS according to its model. This list is based on the circuit shown in Fig. 10. As explained in section III, the variation of the capacitance C_G gives a different value of coupling coefficient (which is a dimensionless quantity) in each position as shown in Fig. 11.

Therefore, the netlist in Spice is going to do a parametric sweep of the capacitance C_G as established in Table II, in this way the motor displacement can be emulated.

With this value of the coupling coefficient, there is a variation in the floating gate voltage, and as shown in Fig. 12, there is no position in which the maximum floating gate voltage ($V_{MAX} = 9.87$ V) is exceeded.

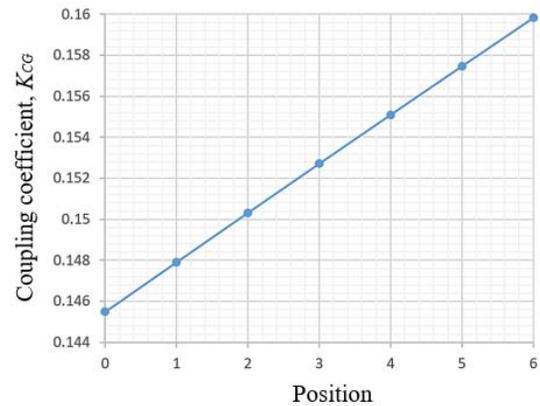


Fig. 11. Variation of the coupling coefficient.

Since this voltage in the floating gate has this variation, the drain current will do the same. As shown in Fig. 13, there is an output curves family of the FGMOS, for each value of C_G that will correspond to a drain current curve, which can be correlated with the position of the micromotor.

The position sensor will have a constant value of drain voltage $V_{DD} = 5V$, therefore the exact values of the currents in each position are shown in Table IV. From this table it can be concluded that the current variation to each step has a value of $7.5\mu A$, this value is measurable and the change in each step can be properly distinguished. The choice of this V_{DD} value was arbitrary considering the operation of the FGMOS in saturation, according to (2), but another value can be chosen as required.

The topologic design was made in L-Edit software using the On-Semi technology of $0.5\mu m$, using N select, Active, Metal1 and Poly1 layer, in order to create the position sensor (Fig. 14).

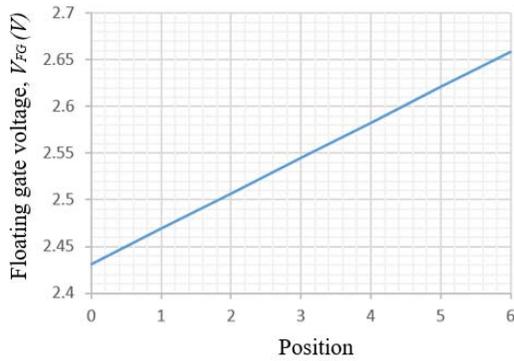


Fig. 12. Floating gate voltage variation.

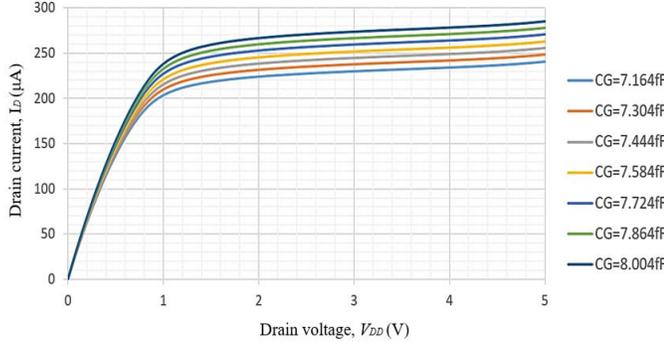


Fig. 13. Current curves in drain.

TABLE IV. CURRENT DRAIN VALUE FOR EACH POSITION

Position	I_D (μA)
Initial (Step 0)	240.54
Step 1	248.04
Step 2	255.52
Step 3	262.99
Step 4	270.44
Step 5	277.88
Final (Step 6)	285.29

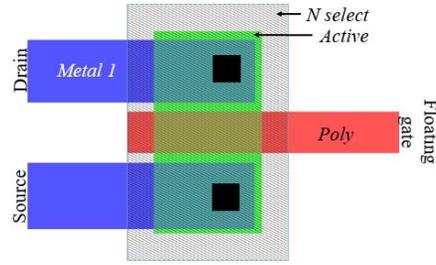


Fig. 14. FGMOS topological design.

V. CONCLUSIONS

Taking into account all the micromotors reported in other works, the research was oriented to achieve the mechanical movement of the micromotor and not to implement a position sensor; however, the design of this micromotor includes a position sensor. One advantage of this sensor is its compatibility with the manufacturing technology of standard CMOS, in which the topological design of all the system could be realized, therefore, it is possible to integrate in the same substrate the structure and the control and sensing position electronics.

Another advantage is that the sensor gives perceptible current measurements using the FGMOS and it can be known in which position the micromotor is.

During the design process, it was very important to take into consideration the maximum floating gate voltage. If this voltage is not exceeded, the physical integrity of the transistor can be maintained. Other consideration was to find a way to integrate the sensor without affecting the mechanical operation of the micromotor.

REFERENCES

- [1] D. Kahng and S. Sze, "A floating gate and its application to memory devices," *The Bell System Technical Journal*, vol. 46, no. 4, 1967.
- [2] C. Bleiker and H. Melchior, "A four-state EEPROM using floating-gate memory cells," *EEE J. Solid State Circuits*, Vols. SC-22, 1987.
- [3] G. Abarca Jiménez, M. Reyes Barranca, S. Mendoza Acevedo, J. Munguía Cervantes and M. Alemán Arce, "Design considerations and electro-mechanical simulation of an inertial sensor based on a floating gate metal-oxide semiconductor field-effect transistor as transducer," *Microsystem Technologies*, 2014.
- [4] G. S. Abarca-Jiménez, J. Mares-Carreño, M. A. Reyes-Barranca and B. Granados-Rojas, "Inertial sensing MEMS device using a floating-gate MOS transistor as transducer by means of modifying the capacitance associated to the floating gate," *Microsystem Technologies*, 2018.
- [5] A. López-Tapia, M. A. Reyes-Barranca, G. S. Abarca-Jiménez, L. Sánchez-Márquez, L. M. Flores-Nava and O. Arellano-Cárdenas, "Design and analysis of the mechanical structure of a linear micromotor based on CMOS-MEMS technology," *International conference in electrical engineering, computing science and automatic control(CCE)*, no. September 11-13, 2019.
- [6] V. H. Ponce Ponce, *Sensor Inteligente de Imágenes en Tecnología CMOS, con Aplicaciones en Robótica*, México: CINVESTAV, 2005.
- [7] A. Lopez-Tapia, *Análisis y diseño de un micromotor lineal basado en tecnología CMOS-MEMS*, México, 2018.
- [8] On-Semi, "Library v57x_rs1 MOSIS wafer electrical tests," On-Semi.
- [9] O. Semiconductor, "C5X 0.5 Micron Technology Design_Rules," 2011.
- [10] J. Baker R., H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation*, New York: IEEE PRESS, 1998.