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Application and Resulting Suitability of a Genetic Algorithm in the Design of FGMOS-based CMOS-MEMS Transducers

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Abstract – In this work an initial approach and requirements overview is performed in order to promote awareness on the compatibility between CMOS – MEMS sensor devices design and the group of heuristic techniques known as genetic algorithms. As might be known, genetic algorithms (GAs) main application is in the field of multivariable functions optimization and this kind of iterative procedures in their simplest forms may be suitable to serve as a tool in the automation of design of integrated CMOS devices and technologies where the variables and restrictions are known. FGMOS-based devices along with MEMS structures when embedded in a single-chip platform (CMOS – MEMS technology) are expected to be in compliance with a set of design rules for both their mechanical and electrical properties, making easier to code and decode variables for their use in a GA in a discrete always-positive basis. In this approach, parasitic and process-resolution-related issues are neglected and further analysis based in a more detailed modeling and parameter restrictions is encouraged.

Keywords – CMOS-MEMS, FGMOS, MEMS, Genetic Algorithm, floating-gate, capacitive MEMS.

I. INTRODUCTION: FGMOS SENSORS REVIEW

As seen in [1] and [2], floating-gate MOS transistors, well known for their charge-based memory-like behavior and capacitive properties, are suitable for the task of transducing the mechanical signal variations, as well as optical [3], chemical [4], etc., into electrical, mostly current-related, easily readable magnitudes.

When it comes to a CMOS – MEMS architecture, especially for the case of capacitive accelerometers, the whole mechanical structure is framed by the many properties and constrains of the CMOS standard technology it is intended for and fabricated in, C5 OnSemi Process for this work.

Elements such as proof masses and beam springs must meet this technology requirements. Beside this, FGMOS-based circuitry and MEMS cells working together are committed to handle signals changing between energy forms from the mere mechanical stimulus to electrical magnitudes. The relation between these two variables is called sensitivity (1) and its optimization is matter of further analysis in this document.

$$S = \Delta X_{out}/\Delta X_{in} \tag{1}$$

Expression (1) is a generally used definition of sensitivity [5] for devices and systems involving MEMS where S might be interpreted as the slope of the transfer function with X_{in} as the input stimuli and X_{out} as a function of X_{in}. Furthermore, in the particular case of accelerometers S_{acc} (or sensitivity of the accelerometer) may be stated as in (2) with a $\mu A/G$ dimension where G is the magnitude of the gravitational acceleration.

$$S_{acc} = \Delta I/\Delta a \tag{2}$$

Fig. 1 provides a schematic of the basic double-gated FGMOS transistor setup coupled to a free-moving capacitance-changing mechanism. In this example the floating gate, which is electrically isolated from other terminals, is induced to a so called *floating* electrostatic potential from two contributions, one of them varying proportionally to the acceleration (and subsequent displacement) in the MEMS structure and another from a conventional floating-gate setup serving as a tuning node for further adjustment of the operation conditions. Drain current can be directly measured or conditioned and transduced from a few μA to about 2V in the drain node as it passes through a series resistor as seen in [6].

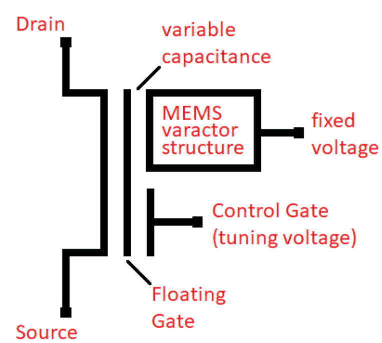

Fig. 1. Basic configuration of the FGMOS-based accelerometer.

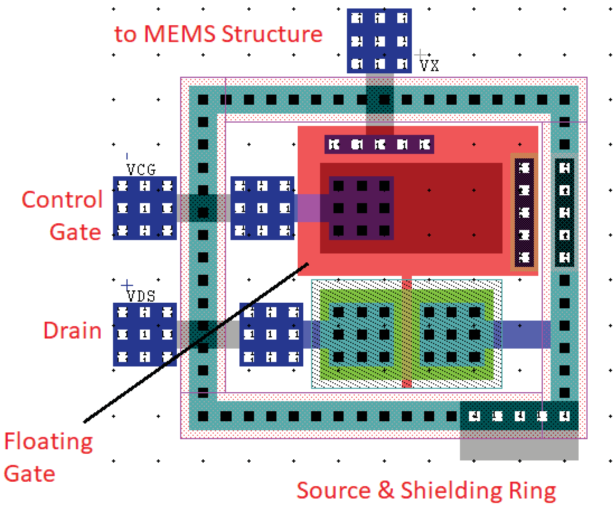

Fig. 2. Layout for a FGMOS in scalable CMOS standard processes.

In Fig. 2 the layout for a conventional floating-gate transistor is depicted. The integrated device contains all of its fundamental terminals including drain, (floating) gate and source plus a control gate and a connection to the capacitive MEMS main structure. As usual in CMOS technology, all of these elements and terminals are defined in terms of a minimum topological unit, a longitudinal parameter called λ which also is the magnitude of resolution for a given technology as all dimensions in the planar design (from a top view) are exact multiples of this minimum step. In the C5 OnSemi Process, commercialized as a $0.5\mu m$ technology, the effective λ is actually $0.3\mu m$, as the name of a CMOS fabrication process is given by a number close to but not necessarily exactly 2λ which corresponds to the minimum channel length of the MOS transistor. Therefore, it is noticeable that every dimension in the topological design, e.g. gate length and width, poly to poly capacitor area's length and width, etc. are an integer multiple of λ so all of these parameters can be coded to and decoded from a binary integer in form of a string L_i bits long. Table 1 summarizes the principal topological variables involved in the basic FGMOS device as long as equation (3) represents the (simplified) transconductive behavior of the conventional MOS transistor in saturation and expression (4) the approximate FGMOS model including the effective floating potential V_{FG} (5) and coupling factor K shown in (6) and neglecting some parasitic capacitance effects.

$$I_D = \frac{W}{L}\frac{KP_n}{2}[V_{GS} - V_{th}]^2 \tag{3}$$

$$I_D = \frac{W}{L}\frac{KP_n}{2}[V_{FG} - V_{th}]^2 \tag{4}$$

$$V_{FG} = \Sigma K_i V_i \tag{5}$$

$$K_i = \frac{C_i}{C_1 + \cdots + C_i + \cdots + C_n + C_{ox}} \tag{6}$$

Where W is the channel width, L is the channel length, K_{pn} is the NMOS transconductance parameter related to electron mobility, V_{th} is the threshold voltage for the MOS transistor, K_i is the couple factor for a given capacitive structure, C_i is the upper capacitive structure, either poly to poly or MEMS for the i-th floating gate and C_{ox} is the gate capacitance below the floating gate. Properties in Table 2 must be taken into account as they are applicable to parameters above in order to meet compliance with the fabrication rules set [7].

Upper limits in Table 2 are strongly limited by the design area (and the budget) but also any device is desired to be "small" so the largest number of test cell may be included in a single-chip project. C_{MS} is directly related to specific proof masses geometries as can be seen in [8] where the dynamic mechanical system is integrated taking advantage of the interconnection metal layers 1, 2 and 3 from the C5 Process [9].

II. BASIC PROPERTIES OF GENETIC ALGORITHMS

Genetic Algorithms and Evolutionary-Computation-related techniques are included in the group of the so called bio-inspired metaheuristic. In general, genetic algorithms are well known as powerful tools to solve linear and non-linear many-variable problems.

Param	Name	Related to:
W	Channel width	oxide capacitance, device transconductance
L	Channel length	oxide capacitance, device transconductance
W_{FG}	Floating gate Poly1 area width	coupling factor, floating potential
L_{FG}	Floating gate Poly1 area length	coupling factor, floating potential
W_{CG}	Control gate Poly2 area width	coupling factor, floating potential
L_{CG}	Control gate Poly2 area length	coupling factor, floating potential
C_{MS}	MEMS Structure Capacitance	mass-spring system displacement, coupling factor, floating potential

Table 1. Design parameters

Param	Minimun	Maximum	Units
W	10	-	$\lambda\ (\mu m)$
L	2	-	$\lambda\ (\mu m)$
W_{FG}	10	-	$\lambda\ (\mu m)$
L_{FG}	10	-	$\lambda\ (\mu m)$
W_{CG}	6	-	$\lambda\ (\mu m)$
L_{CG}	6	-	$\lambda\ (\mu m)$
C_{MS}	-	-	$\sim fF$

Table 2. Feasibility due to fabrication limitations.

Even in its simpler form a GA can, with relative ease, handle optimization problems with more than a hundred variable parameters. Most of the proposed models and objective functions $f(x_1, \dots, x_n)$ to analyze in a computer science environment are especially designed as benchmarks and are not necessarily representing a real-world problem. Engineering conventional problems usually include a few dozens of variables. In this context, one variable corresponds to one gene, and gathering all the variables together is similar to have a chromosome with every aspect of the solution within.

As expected, a GA is a computational interpretation of how across the generations the information in DNA adapts itself to fulfill as much as possible the problem's best solution, that said, the implementation in hardware and/or software requires of a group of considerations which include but is not limited to:

1. A *representation* method: a mechanism to code a group of numerical variables of any kind to a composite of data, usually a single binary string as seen in Fig. 3, and decode it back.
2. A *selection* method: a strategy to pick one or more solutions of many possible (the population) to assign them privileges, penalization or to perform operations between them.
3. Modeling of the *crossover* (recombination) of two solutions, also called individuals: A procedure to recombine them looking for an even better solution. A high crossover rate controlled by a crossover probability $P_C > 0.5$ is desirable as its effect resembles the interpolation process.
4. Modeling of *mutation*: Randomly changing some of the values in the coded strings. A low mutation probability $P_M < 0.1$ is desirable to ensure diversity among the population without affecting the convergence tendency to optimal solutions.
5. Modeling of *elitism*: A mechanism to ensure the survival of the best individuals from a given generation to the next.

Is not subject of the present work to deeply analyze the complex theoretical issues, advantages and drawbacks of GA's but to overview the MEMS-oriented FGMOS design from that point of view. Previous works in related fields such as [10], [11] and [12] fields have successfully translated philosophy of evolutionary computation to MEMS design.

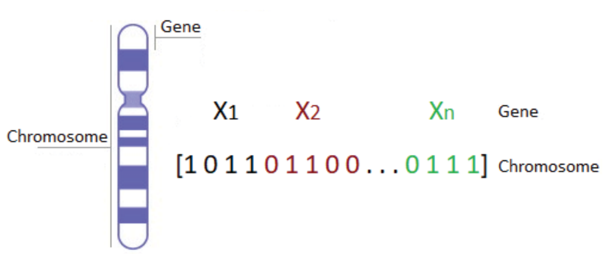

Fig. 3. Gene and chromosome interpretation.

We point out that most of microelectromechanical systems are actually developed and fabricated in dedicated MEMS technologies with a variety of rules and tolerances others than those available in CMOS – MEMS joint technology and process. The pseudocode shown below, in terms of a population P is a genetic algorithm based on the ideas proposed by Holland in 1975 [13] and the one this work takes as an example.

```
t ← 0;
initialize (P(t = 0));
evaluate(P(t = 0));
while is NotTerminated()
do {
        P_p(t) ← P(t).selectParents();
        P_c(t) ← reproduction(P_p);
        mutate(P_c(t));
        evaluate(P_c(t));
        P(t + 1) ← buildNextGenerationFrom(P_c(t), P(t));
        t ← t + 1;
   }
end
```

During the execution of this algorithm we may pay special attention to the historical values of fitness of every member of the population so convergence mechanisms, such as elitism, can be implemented. The fitness value of an individual comes from evaluating a dedicated function carefully designed to represent compliance with the optimization objectives.

III. VARIABLES REPRESENTATION AND TESTING

As seen in [8], capacitance values for a CMOS – MEMS structure designed and built in a comprehensive area can reach about $5fF$ in non-accelerated conditions $(a = 0)$ and variation up to $1fF$ in $a = g$. Combining these results with expressions (3-6), drain current of the FGMOS is obtained (7).

$$I_D = \frac{W}{L}\frac{KP_n}{2}\left[\left(\frac{C_{MS}}{C_{MS}+C_{CG}+C_{ox}}V_{MS} + \frac{C_{CG}}{C_{MS}+C_{CG}+C_{ox}}V_{CG}\right) - V_{th}\right]^2 \tag{7}$$

Where K_{pn} and V_{th} are constants for the fabrication process and its base technology, C_{CG} and C_{ox} are in terms of W and L and V_{MS}, V_{CG} are source supplied voltages others than V_{DD} that can be proposed or calculated even during the GA itself. Assuming C_{MS} to be fairly linear and proportional to displacement y in [8], we can redefine (2) as (8) and (9) and look for an optimal combination of parameters W, L, W_{FG}, L_{FG}, W_{CG}, L_{CG}, V_{MS} and V_{CG} that maximizes S_{acc} regarding (10).

$$S_{acc} = \frac{\partial I_D}{\partial C_{MS}} \tag{8}$$

$$\frac{\partial I_D}{\partial C_{MS}} = \frac{WKP_n}{L}\left(\frac{V_{MS}C_{MS}+V_{CG}C_{CG}}{C_{MS}+C_{CG}+C_{ox}} - V_{th}\right)\left(\frac{V_{MS}C_{CG}+V_{MS}C_{ox}-V_{CG}C_{CG}}{(C_{MS}+C_{CG}+C_{ox})^2}\right) \tag{9}$$

$$C_i = \frac{\epsilon_r\epsilon_r A_i}{d} = \frac{3.9\epsilon_r W_i L_i}{t_{ox}} \tag{10}$$

var	min	max	codec	length
W	10	50	$(n-10) \leftrightarrow gray$	6 bits
L	2	10	$(n-2) \leftrightarrow gray$	4 bits
W_{FG}	10	40	$(n-10) \leftrightarrow gray$	5 bits
L_{FG}	10	40	$(n-10) \leftrightarrow gray$	5 bits
W_{CG}	6	30	$(n-6) \leftrightarrow gray$	5 bits
L_{CG}	6	30	$(n-6) \leftrightarrow gray$	5 bits
V_{MS}	0.01	3.30	$(m-1) \leftrightarrow gray$	9 bits
V_{CG}	0.01	3.30	$(m-1) \leftrightarrow gray$	9 bits

Table 3. Variables codification.

For the purposes of applying the GA, every variable parameter must be coded into a binary string according to their range and desired resolution. Table 3 summarizes the codification characteristics. All strings corresponding to each variable are concatenated into a single string with a total of 48 bits, where n is the number of times to multiply the layout resolution λ for a given length and m is a multiple of $0.1V$ as well. Evaluation of this 8-variable for all allowed combinations would generate a matrix with about 24 trillion values, so that a direct search method for maxima is not convenient.

The GA was implemented and tested for 1000 generations and varying between populations of 100 and 200, crossover probabilities of 0.6, 0.7 and 0.8 and mutation probabilities of 0.01 0.05 and 0.1. As expected, higher mutation rates and larger populations keep mean fitness lower. In terms of the GA, the procedure included single-point crossover, death penalty (fitness = 10) for infeasible individuals and integration of the elitist individual within the next generation. Three of the executions with the highest fitness function evaluation are shown in Fig. 4, Fig. 5 and Fig. 6 (mean fitness dashed line).

Resulting parameter values leads to a drain current I_D in the FGMOS in the order of $200\mu A$ which is suitable to work with the integrated amplifier proposed in [6]. Table 4 reports average parameter results.

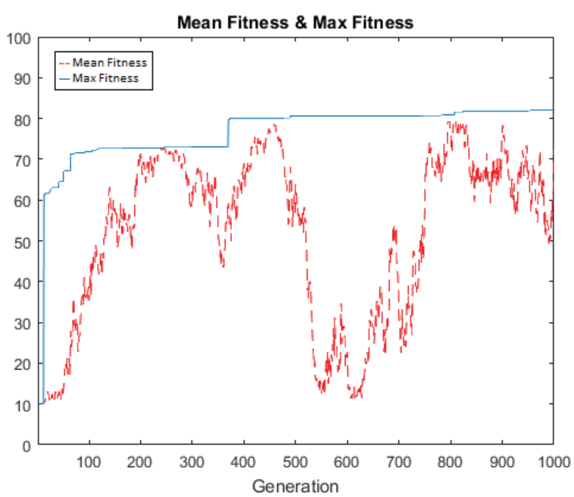

Fig. 4. Pop: 100, Pc: 0.7, Pm: 0.01, maxfitness: 82.22, average fitness in the population presents large variations across generations.

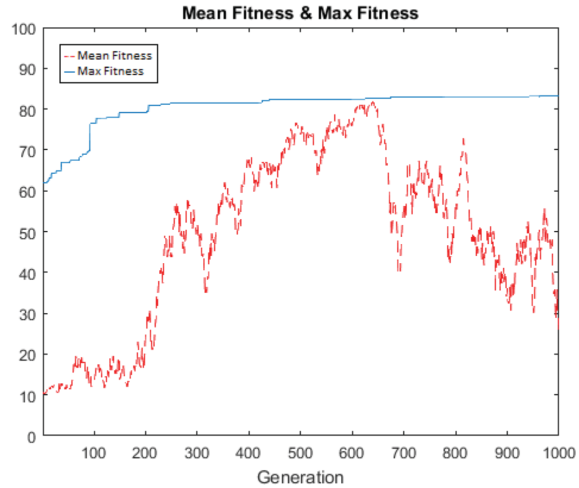

Fig. 5. Pop: 200, Pc: 0.7, Pm: 0.01, maxfitness: 83.19. Mean fitness settles a mid-range indicating more diversity among individuals in the population.

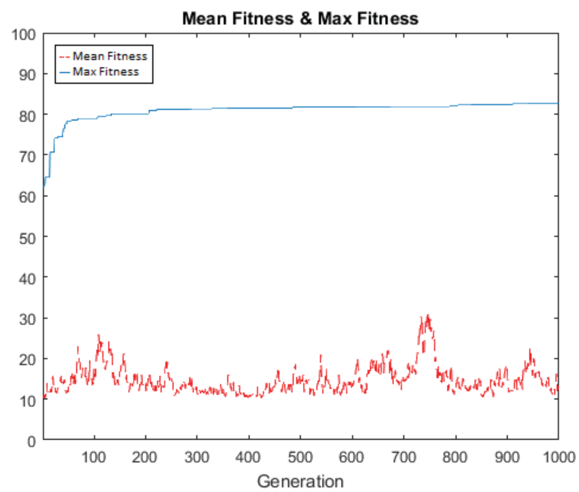

Fig. 6. Pop: 200, Pc: 0.8, Pm: 0.05, maxfitness: 82.71. At higher mutation fast convergence issues may appear even when the mean fitness stays low, this is critical when it comes to a problem with many local optimal points.

var	min	max	computed (avg)	units
W	3	15	12	μm
L	0.6	3	0.6	μm
W_{FG}	3	12	9.9	μm
L_{FG}	3	12	6.9	μm
W_{CG}	1.8	9	5.4	μm
L_{CG}	1.8	9	2.4	μm
V_{MS}	0.01	3.3	3.3	V
V_{CG}	0.01	3.3	3.3	V

Table 4. Computed parameters.

IV. CONCLUSIONS

Knowing genetic algorithms nowadays are capable of solving way harder computational problems, this exercise is not intended to represent any advantage more than adding an automation and design validation tool to the analysis of FGMOS-based CMOS-MEMS devices.

Since a few of the computed parameters settled down to extreme values within their allowed ranges, it is convenient to revisit how the contribution of them affects to the global model, not discarding the possibility to take one or more of these variables down to their most fundamental modeling, deeply related to the physical process that take place to form the transistor. The optimization and design automation of complex digital and mixed-signal systems where the application itself is bio-inspired might be challenging and a fertile research field.

A major suitability advantage we identified and reason to keep GA's in mind, is related to memory handling for the variables and the computational cost of a direct search method. Even if this single-transistor example were reduced to 5 or 6 variables, the search space is so big, such that a direct search method would require instances larger than hundreds of megabytes to be computed. In the other hand, a typical execution of the basic GA with a random initial population of about 100 individuals is expected to last no longer than a couple of minutes.

We assume fairly convenient to take advantage of the perspective and philosophy of GA's from which we highlight the codification process that allowed us to work on the solution in a different space other than the conventional VLSI design. This vision might be complemented with a solid knowledge in other bio-inspired metaheuristics.

V. FUTURE WORK

As summarized in the conclusions of this work, a way to find new features and put to the test the compatibility of GA's and CMOS – MEMS design, is to evaluate circuit models way higher in complexity, where up to a few hundreds of variables and parameters shall be resolved to their optimal values.

Might be interesting to link the MEMS and VLSI design duties with combinations of GA's and other heuristics such as Fuzzy Logic and Artificial Neural Networks in order to obtain the optimal parameters knowing not the mathematical model but the desired behavior.

Investigation on hardware implementation (HDL) and its automated translation to CMOS layout is also desirable.

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REFERENCES

[1] G.S. Abarca-Jiménez, M. A. Reyes-Barranca, et al. "MEMS Capacitive Sensor Using FGMOS." 2013 10th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE), 2013

[2] G. S. Abarca-Jiménez, M. A. Reyes-Barranca, et al. "Modal analysis of a structure used as a capacitive MEMS accelerometer sensor." 2014 11th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE), 2014

[3] S. Domínguez-Sánchez, M. A. Reyes-Barranca, et al. "A Prototype Design for an Accelerometer Using a Multiple Floating-Gate MOSFET as a Transducer." 2014 11th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE), 2014

[4] S. Mendoza-Acevedo, M.A. Reyes-Barranca, "Study for the micro-machining optimization of micro hotplates used in MEMS-CMOS gas sensors." 2011 8th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE), 2011

[5] Kaajakary, Ville. (2009). Practical MEMS. Small Gear Publishing, p. 170.

[6] B. Granados-Rojas, M. A. Reyes-Barranca, et al. "Basic readout circuit applied on FGMOS-based CMOS-MEMS inertial sensing prototypes." 2017 14th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE). 2017

[7] ON Semiconductor. C5X, 0.5 Micron Technology Design Rules 4500099 Rev. X, 2011.

[8] B. Granados-Rojas, M. A. Reyes-Barranca, et al. "3-layered Capacitive Structure Design for MEMS Inertial Sensing." 2016 13th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE). 2016

[9] ON Semiconductor. C5X, 0.5 Micron Technology Design Rules 4500099 Rev. X, p. 99., 2011

[10] I. Darnobyt, R. Kryvyy, et al. "Possibilities of the use of genetic algorithms in design of MEMS elements" 2008 International Conference on Perspective Technologies and Methods in MEMS Design. 2008

[11] R. Kryvyy, M. Lobur, et al. "Factors of influence on genetic algorithm's work in MEMS design" 2009 10th International Conference - The Experience of Designing and Application of CAD Systems in Microelectronics. 2009

[12] M. Melnyk, A. Kernytskyy, et al. "Application of a genetic algorithm for dimension optimization of the MEMS-based accelerometer" Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2013

[13] Holland, John H. (1975). Adaptation in Natural and Artificial Systems. The University of Michigan Press.