Electronic architecture for an analog retinal processing prototype suitable to be implemented on standard CMOS technology

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Abstract — **An analog architecture of optic signal processing is presented in this work, with the goal to emulate one of the much processes involved in a biological retina. Here we have considered that the receptive field is the main unit of processing in the visual system. So, the proposed architecture tries to give partial solution to the properties of a receptive field in order to give some help to people with retinal diseases in the future. A receptive field is represented by an array of 3x3 pixels and four main mathematical operations are carried out on each one pixel. This means that image processing is developed at pixel level. Operations involved are: (1) photo-transduction by photocurrent integration; (2) Average of the signals coming from the eight neighbouring pixels, obtained by a neu-NMOS (ν-NMOS) neuron; (3) The gradient between central pixel and the average value from neighboring pixels. This operation is done by a comparator; (4) a generator of impulses whose density is proportional to the gradient. The coupling methodology among every block or module, and the PSPICE simulation using the technology parameters of 0.5μm are the main objectives in this work.**

Keywords — **Receptive fields, analog signal processing**

I. Introduction

The main characteristics of the retina´s receptive field were reported recently [1]. They are summarized in Table 1. Particularly, this work will deal with the design of the so called "ON" center with sustained and transient response. Properties of these kinds of receptive fields are illustrated in Fig. 1. There, two opposite conditions are shown, i.e. one when just the center is illuminated and other when just the surround is illuminated. However, in practice whether the center or the surrounding of a receptive field is more illuminated, can be determined through gradient computations, in a wide continuous range of illumination.

TABLE 1
TYPE OF RECEPTIVE FIELD

RECEPTIVE FIELD	TYPE OF RESPONSE
"ON" Center with	Sustained Response
	Transient Response
"OFF" Center with	Sustained Response
	Transient Response

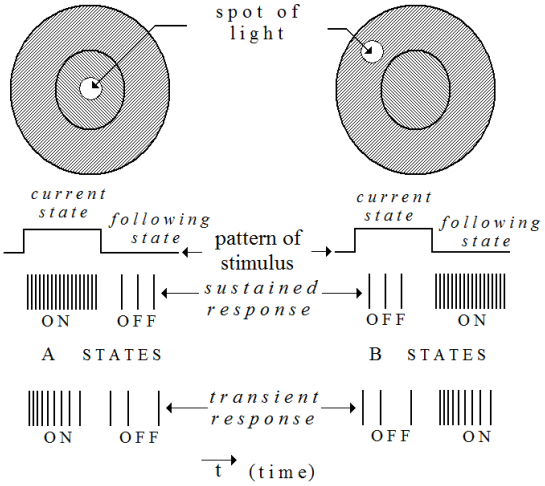

Fig. 1. The main properties of the "ON" center with sustained and transient response.

The model was reported in a previous work [1]. Regarding biological threshold of a neuron (δ), if the firing threshold $\delta > 0$, then the model's behavior is summarized in Table 2. In this Table, Δv_{AVE} represents the average gradient between the center and the surroundings of the receptive field. Hence, these alternatives will be explained.

TABLE 2
SUMMARIZED MATHEMATICAL MODEL OF NEURON RESPONSE

CONDITION	RESPONSE
$\Delta v_{AVE} > \delta$ center with highest illumination	$f_{on} = K_{ons}^{+} \cdot \Delta v_{AVE}$ sustained response "A-STATE"
$\Delta v_{AVE} < \delta$ center with lower illumination	$f_{off} = K_{ons}^{-} / \Delta v_{AVE}$ Sustained Response "A-STATE"
$\Delta v_{AVE} > \delta$ center with highest illumination	$f_{ont} = f_{on} \cdot exp(-K_{12} \cdot t)$ Transient Response "A-STATE"
$\Delta v_{AVE} < \delta$ center with lower illumination	$f_{offt} = f_{off} \cdot exp(-K_{22} \cdot t)$ Transient Response "A-STATE"

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The other quantities in Table 2 are: f_{on} is the response that belongs to the A-STATE sustained receptive field type (current state) with $\Delta v_{AVE} > \delta$ (Fig 1). f_{off} is the response that belongs to B-STATES sustained receptive field type, (current state) with $\Delta v_{AVE} < \delta$ (Fig. 1). A similar description can be done for transient responses f_{ont} and f_{offt} respectively in Table 2 and Fig. 1. K_{ons}^{+} and K_{ons}^{-} are proportionality constants and K_{12} and K_{22} are time constants.

II METHODOLOGY

From conditions given in Table 2 and considering the analog processing in biological neurons, a model is proposed which is based on the gradient between a center and the surroundings of the receptive field. Analog and local processing at pixel level are here the main approaches in order to avoid as much as possible separated and external components to the internal chamber of the eye, and also to emulate as closely as possible the biological processing of vision. The architecture here proposed and analyzed was generated and supported by mathematical models as those shown in Table 3. Also, a receptive field is emulated by a 3x3 array of pixels such as is shown in Fig. 2.

Each pixel has four operator modules which have been generated from the equations in Table 3. The central pixel represents the center of the receptive field and the other eight neighbor pixels represent the surrounding. Fig. 3 shows the general architecture in a block diagram, according to a top-down methodology. The coupler modules, adjusts the respective levels of voltage, in both cases either between the ν-NMOS and the comparator modules or between the comparator and the oscillator modules (Fig 3). So, a pixel with a general architecture as that displayed in Fig. 3 emulates a ganglion cell neuron in the retina.

TABLE 3

ASSOCIATED SUB-CIRCUITS FOR EACH MATHEMATICAL OPERATION

MATHEMATICAL MODEL	ASSOCIATED SUB-CIRCUIT
$V_{AVE} = \frac{1}{8}\sum_{k=1}^{8} V_k$	Operation carried out by a ν-NMOS neuron, shown in Figs. 3 and 4
$\Delta v_{AVE} = V_C - V_{AVE}$	Achieved by a dynamic comparator, shown in Fig. 3
$f_{ont} = f_{on} \cdot exp(-K_{12} \cdot t)$	Low frequency Voltage-Controlled Oscillator for pulsed generator, given in Fig. 3
$\Delta V_{ph} = \frac{1}{C_{ph}} \cdot i_{ph} \cdot \Delta t$	Integration carried out by a photo-transducer module, shown in Fig 3

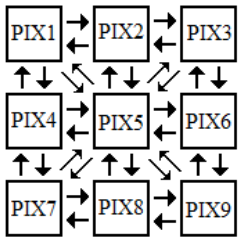

Fig. 2. Architecture of a Receptive Field

Quantities in Table 2 are: V_k is the *k-th* value set of the neighbor pixels in the surrounding of receptive field, including the central pixel (PIX5 in Fig. 2). V_{AVE} is the arithmetic average value in neighbor pixels. V_C is the central pixel value. The photocurrent is denoted by i_{ph} and the parasitic capacitance by C_{ph} which integrates photocurrent as photo-voltage ΔV_{ph}, by assuming that i_{ph} is constant during time. To understand the way in which the proposed architecture operates, each of its main modules (Table 3) will be explained in the following sections based in the architecture shown in the Fig. 3.

A).- *CMOS architecture for the ν-NMOS neuron*:

1).- Analysis of input variables of the ν-NMOS neuron

The operation of the ν-NMOS neuron is based on the operation principles of a FGMOS transistor [2]. However, this is not exactly a FGMOS transistor, but a *quasi-floating gate* MOS transistor [3-4]. This means that the gate made with Poly1 is not floating, on the contrary, it is connected to an external DC level V_{ADJ}. This is shown in Fig. 4. Eight external inputs (Control Gates, Poly2), labeled as $V_1, V_2, \cdots, V_8$, are capacitively coupled to Poly1 gate. The purpose of the external connection to the Poly1 layer is to adjust the offset of V_{OUT} in node 2 indicated in Fig. 4, by adjusting V_{ADJ}. The input potential in the quasi-floating gate of the ν-NMOS transistor is given by equation (1).

$$\Phi_{IN} = v_{IN} + V_{INoffset} \quad (1)$$

Where:

$$v_{IN} = \frac{C}{\delta_f \cdot C_T}\left(\sum_{k=1}^{8} V_k\right) \quad (2)$$

and

$$V_{INoffset} = \gamma_{gd} V_{DD} + \gamma_{gs}\left(a_m \cdot V_{ADJ} - V_{TH}\right) \quad (3)$$

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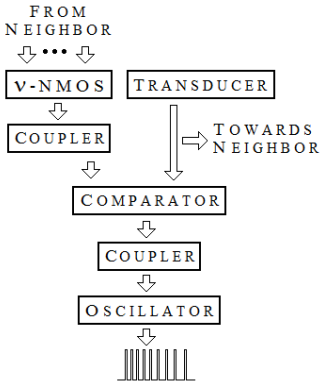

Fig. 3. Pixel's Architecture

with $\gamma_{gd} = \frac{C_{gd}}{\delta_f \cdot C_T}$ and $\gamma_{gs} = \frac{C_{gs}}{\delta_f \cdot C_T}$ being the coupling coefficient for the parasitic capacitances *Gate-Drain*, gd, and *Gate-Source*, gs, respectively. The input signal v_{IN} is the weighted average due to the input from neighboring pixels. So the arithmetic average $\frac{1}{8}\sum_{k=1}^{8} V_k$ is mapped to $\frac{C}{\delta_f \cdot C_T}\left(\sum_{k=1}^{8} V_k\right)$ by the ν-NMOS neuron. Here δ_f is the feedback coefficient between the input and the output through the parasitic capacitance C_{gs}. Assuming that each Control Gate has the same size, then C is the coupling capacitance between the Control Gates and Poly1, and C_T is the sum of all capacitances, including parasitics.

2).- Analysis of output variables in the ν-NMOS neuron

V_{OUT} is the neuron's response and is modeled by

$$V_{OUT} = m_p \cdot \Phi_{IN} + V_{OF} \quad (4)$$

And it output is shown in the Fig. 4. V_{OF} is an offset level at the output of ν-NMOS neuron and m_p is simply a proportionality constant, considering that the neuron is an electronic circuit configured as a non ideal source follower.

B).- *Photo-transducer for sustained response*

In the case of the photo-transducer, its schematic diagram is shown in Fig. 5. The integration time is controlled by VSHU applied to the gate of MSHUT and the reset time is controlled applying VRE to the gate of MREST. The role of Mdum is to minimize the digital noise introduced through VSHU and VRE. V_{outph} is the output of the photo-transducer which is expressed as:

$$V_{outph} = V_{offsetph} + \Delta V_{ph} \quad (5)$$

Where $\Delta V_{ph} = \frac{1}{C_{ph}} \cdot i_{ph} \cdot \Delta t$ (6)

ΔV_{ph} falls between the limits:

$$V_{rest} < \Delta V_{ph} < V_{DD} \quad (7)$$

and it can be assumed that inside this window i_{ph} is constant in time, for a given illumination value. One of the most important features in the architecture of the photo-transducer is that the stored potential at node N2 is sustained because it is floating when MSHUT is open across the reading phase. So we call this the sustained response.

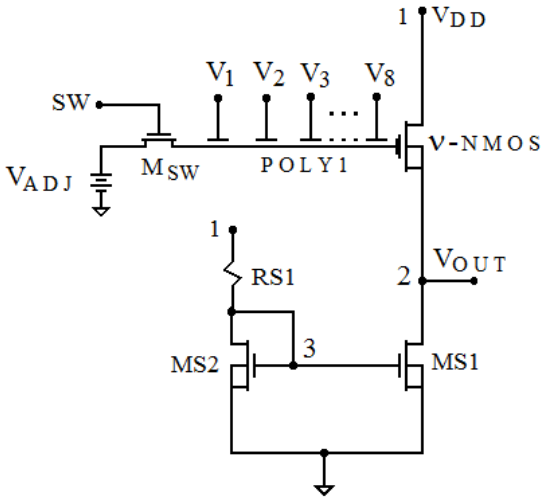

Fig. 4. Schematic diagram for the complete ν-NMOS

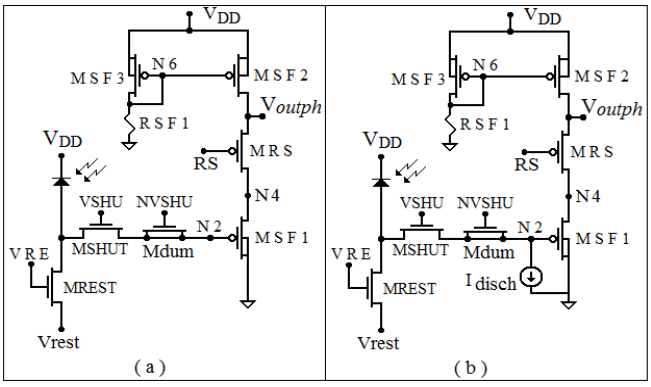

Fig. 5. Schematic diagram of the photo-transducer for (a) sustained (b) transient response respectively

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C).- *Photo-transducer for transient response*

Since node N2 in Fig. 5(a) sustains the potential stored while MSHUT is open (reading phase), a discharge can be produced in this node in order to obtain a transient condition. This can be carried out by means of a current source I_{disch} of the order of pA, Fig. 5(b). It is connected between node N2 and ground. Therefore I_{disch}, produces a discharge at node N2. The discharge time is a function of the value of I_{disch} (usually in the order of pA). This way, control can be established for the discharge during the reading phase. This behavior can be modeled with:

$$V_{outph} = V_{offsetph} + \Delta V_{ph} \cdot exp(-k \cdot I_{disch} \cdot t) \quad (8)$$

which is the same model as that given by the third equation in Table 3. $V_{offsetph}$ is simply an offset level.

D).- *Comparator*

The schematic circuit of the comparator is shown in Fig. 6. In regard to the comparator, it should have some main features such as the followings: I) for each value of V_{OUT} a transfer function like that shown in Fig. 7 will result. II) Furthermore if $V_{outph} > V_{OUT}$, the value of V_{out-c} (see Fig. 6) would be a high analog value. III) If both, V_{outph} and V_{OUT} are small values, which represents a low illumination condition, then V_{out-c} will have a low value. IV) Finally, if both, V_{outph} and V_{OUT} have high values, which represents a high and uniform illumination condition, then V_{out-c} will have an intermediate value, not too high and not too low. These are features needed for a dynamical comparator. The last three features are not shown in Fig. 7. As it can be seen in Fig. 6, the comparator is designed with two mutually controlled current mirrors, one of them operating as a current sink and the second as a current source. The properties, I), II), III) and IV) previously specified are satisfied by the architecture of the comparator given in the Fig. 6.

Next, the second expression in Table 3 can be rewritten with new subscripts related now to the notation used in the schematic circuits, this is:

$$V_{out-c} = V_{outph} - V_{OUT} \quad (9)$$

with $V_{out-c} \equiv \Delta v_{AVE}$, however, it should be considered that if $V_{outph} > V_{OUT}$ then:

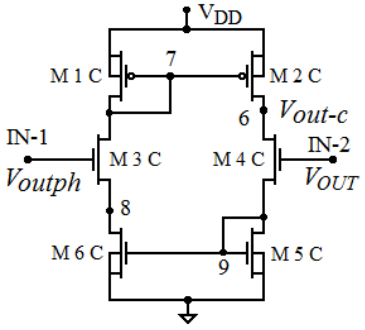

Fig. 6.- Schematic circuit of the comparator

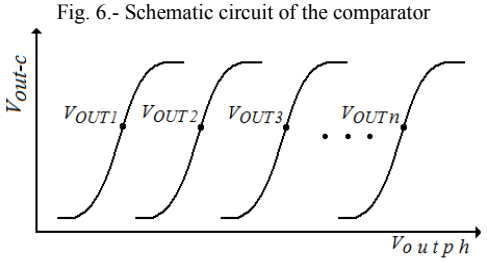

Fig. 7. Transfer function of the comparator

$$V_{out-c} = V_{outph} - V_{OUT} \quad (10)$$

From this last consideration, if both V_{outph} and V_{OUT} have small values, then V_{out-c} has a small value. That corresponds to a low illumination condition. Moreover, if $V_{OUT} > V_{out-c}$ then $V_{out-c} \rightarrow V_{small}$ which means that V_{out-c} tends to a small value. Then in turn, the neuron's response can be smaller than the neighbors' response if it is placed in the center of a receptive field.

E).- *Oscillator*

Two important features can be enhanced: first, it can operate with frequencies below 10kHz. It should be remembered that biological neurons work at very low frequencies (10Hz to 1kHz). The second important feature is that the pulse width fits to 100μs. The oscillator is a voltage-controlled and its general architecture is shown in Fig. 8.

The core oscillator in Fig. 8 is able to generate pulses at low frequencies. Actually, each of the so called "*differential pair*" is not an exactly symmetrical pair since the difference between the aspect ratio of the input transistors is designed to produce an unbalanced condition resulting in oscillations. Frequency is adjusted with the voltage INOSC which is the output from the comparator. Oscillation is produced due to the difference in aspect ratios of M2 and M3. By adjusting the aspect ratio of M4 and M5 the pulse width can be controlled. For the case of sustained response the frequency is given by:

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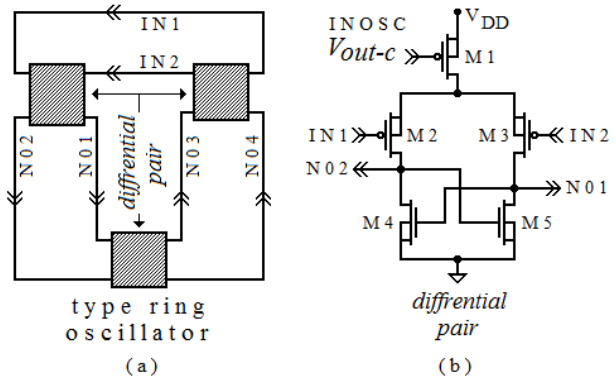

Fig. 8.- Oscillator's architecture

$$f_{on} = K_{ons}^{+} \cdot \Delta v_{AVE} \qquad (11)$$

This is the model for the response of the oscillator when it is excited with the circuit shown in Fig. 5(a). On the other hand, if the oscillator is excited with the circuit shown in Fig. 5(b) the response will be transient and this is modeled by equation (12).

$$f_{ont} = f_{on} \cdot exp(-K_{12} \cdot t) \qquad (12)$$

Here $\Delta v_{AVE} = V_{out-c}$ is evaluated by the comparator.

III. Results Of Simulations

1).- *Results for the ν-NMOS neuron*:

An important and useful stage in the design of any integrated circuit is the circuital simulation. This is the main goal in this report. Following, simulations will be presented for each module described before. First Fig. 9 shows the transfer function of a neuron ν-NMOS.

Fig. 10 shows the floating-gate voltage of a ν-NMOS as a function of one of the eight control gates, V_1, keeping the other seven inputs to ground, with V_2 as a parameter. We can see from Figs. 9 that if V_{ADJ} = 1.6V the output from the ν-NMOS transistor is almost 0.56V. That means that when the weighted inputs V_3, …, V_8 are above V_{TH} the neuron is fired. So, we can adjust V_{ADJ} in order to obtain an output purely due to weighted inputs. For example, V_{ADJ} could take values from 1.0V to 3.0V, according to the simulation shown in Fig. 9. On the other hand, capacitances C, and C_T as well as the constant δ_f are experimental values and can be evaluated in a future work. However, from the simulated data in the Fig. 10, it was possible to estimate the number $C/(\delta_f \cdot C_T)$ having values ranging from 0.07 to 0.1 which is very near to 1/8, a value given in the first model in the Table 3. Simulations were carried out by using model reported in [5].

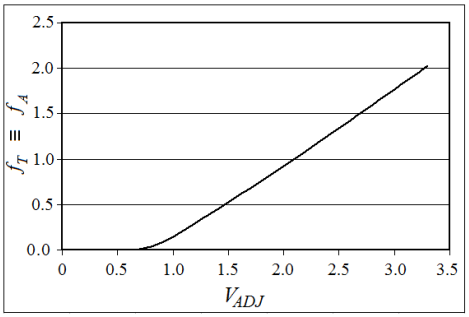

Fig. 9.- Transfer Function of a neuron ν-NMOS by sweeping V_{ADJ}

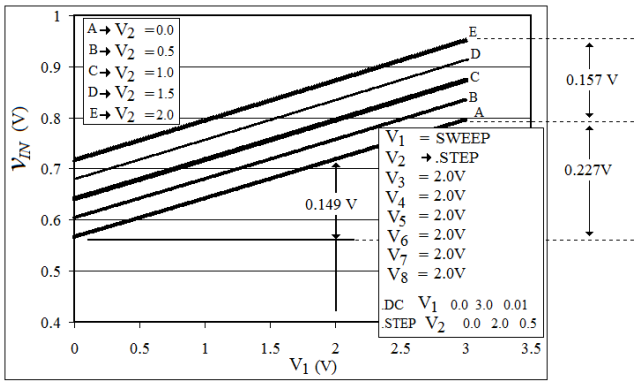

Fig. 10.- Response from a neuron ν-NMOS with no physical connection of the floating-gate (Poly1 layer).

2).- *Results for the transducer*:

From Figs. 5 (a) and (b), the photodiode's cathode has a highest voltage than its anode at the beginning of the integration time. Hence, due to the leakage current the node N2 tends to reach the voltage at node V_{DD}, namely, the voltage at node N2 grows from the level of V_{rest} to the level of V_{DD} during the integration time. Since the transducer is a source follower its output is expected to be near the value present in node N2. Figs. 11 and 12 show this behavior. During the Reset-Time, node N2 is set to Vrest, then the Integration-Time starts. After this period is the Hold-Time, where reading or processing is carried out.

3).- *Results for the Comparator*:

The voltages v_{IN} and V_{outph} from the neuron ν-NMOS and the transducer, respectively, are inputs of the comparator. The performance from the results of the simulations is shows in the Fig. 13. According to Fig. 13, when $V_{outph} > V_{OUT}$ the response will be high. The better example is the graphic number 6. If $V_{OUT} > V_{outph}$ the response always is low and the better example is the graphic

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number 0. When both, V_{outph} and V_{OUT} are low values, which belong to low illumination, the response is low.

IV. Conclusions

Finally, simulations for the pixel array shown in Fig. 2 were carried out, including the performance evaluation of the oscillator, giving excellent results, some of them are shown in the Fig. 14. That figure presents the response when neighbor pixels deliver 20pA and the central pixel delivers 40pA, with an integration time of 14ms. These data belong to a low illumination condition. On the other hand, a retinal prosthesis requires a methodological process in order to get feasible results which can be implemented on silicon with a standard technology. So, in this work we have presented the stage of simulation. The main contribution of this work is proposed methodology for the analog processing that will give a response for optical devices in order to emulate the biological response of those neurons called "ganglion cells" in the retina. This work represents the stage of simulation, inside a methodological process in the building of a prototype for a retinal prosthesis. The core of analog processing is the ν-NMOS artificial neuron.

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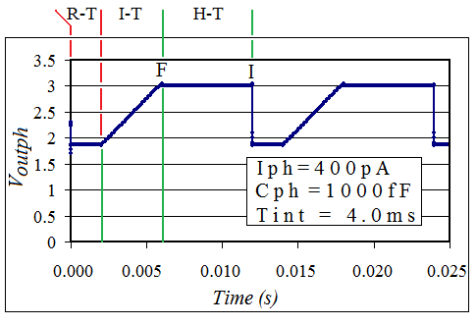
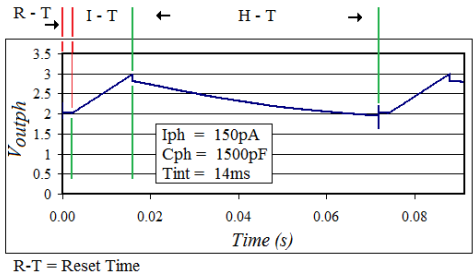


R-T = Reset Time
I - T = Integration time
H-T = Hold Time

Fig. 11.- Domain Time Transducer for Sustained Response



R-T = Reset Time
I - T = Integration time
H-T = Hold Time

Fig. 12.- Domain time Transducer for Transient Response

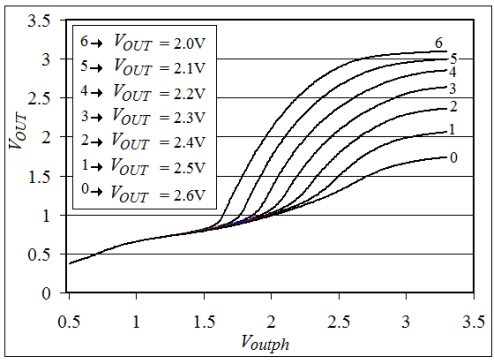


Fig. 13.- Parametric transfer function comparator

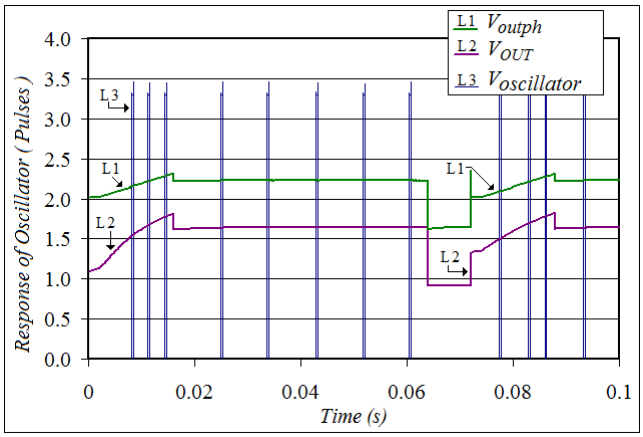


Fig. 14.- Receptive Field With Sustained Response

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