# New Trends in Electrical Engineering Automatic Control, Computing and Communication Sciences

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**José Antonio Moreno Cadenas**
*To Zuleima and Darien*
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# Preface

This book contains extended versions of selected papers presented at the *2008 5th International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE'2008)*, which took place in Mexico City, México during 12–14 November, 2008.

This volume contains 28 chapters organized in four parts, each of them corresponding to one of the major topics covered in CCE'2008. Next, we provide a short description of each of these 28 chapters.

Part I contains the following 10 chapters related to automatic control and mechatronics:

In chapter 1, Lu investigates mixed finite element methods for semilinear optimal control problems. The author derives *a priori* error estimates for the coupled state and control approximation, and presents a numerical example that confirms the author's theoretical results.

Robles-Aguirre et al. present in chapter 2, the design of first and second order sliding mode controllers for the synchronous generator speed, Unified Power Flow Controller (UPFC) series power flows, UPFC voltage magnitude and UPFC internal DC link voltage. The authors use combinations of sliding mode and block control techniques to design these controllers, which are implemented in a small power system. Digital simulations are adopted by the authors to illustrate the effectiveness of the proposed approach.

Chapter 3, by Garrido and Miranda, presents a method for DC servomotors working in a closed loop. They use a proportional integral controller to stabilize the servomotor, and another one to close the loop around a linear model of the servomotor. A laboratory prototype is used to validate the proposed method.

In chapter 4, Villafuerte and Mondié propose a new approach for the analysis of the case of neutral and retarded type time delay systems. Some examples and a case study are adopted to illustrate the proposed approach.

Galvan-Guerra and Azhmyakov consider, in chapter 5, the linear quadratic impulsive hybrid optimal control problem and apply to it the corresponding Pontryagin-type maximum principle. The aim of the authors was to investigate the relationship between such a maximum principle and the Bellman dynamic programming approach. They also formulate the necessary optimality conditions for the problem of their interest and derive the associated Riccati-type equation, which allows an implementable numerical algorithm.

Chapter 6, by Garrido et al., presents a task-space controller for robot manipulators, which uses two proportional actions at joint and task levels. Such a topology exploits the fact that, in general, measurements at the task level are noisier than the measurements at the joint level. A planar 2-link revolute joint robot under visual feedback is used by the author to assess the performance of the proposed approach.

Sánchez and Collado propose in chapter 7, a modified version of the standard truncated Carleman linearization, which reduces the error in the truncation process. This modified approach is applied to two Van der Pol oscillators with slightly different frequencies.

Arias-Montiel and Silva-Navarro present in chapter 8 a LQR control scheme for unbalance compensation using an active magnetic bearing in a rotor-bearing system. Simulation and experimental results are included in the chapter to show the transient and steady-state behavior of the proposed closed-loop system.

In chapter 9, Cabrera-Amado and Silva-Navarro address the problem of unbalance compensation in a rotor-bearing system. The authors apply a semiactive balancing control scheme based on two radial MR dampers mounted in one of the supports. Some numerical simulations and experimental results on a physical platform are presented to validate the dynamic and robust performance of the proposed control system.

Finally, in chapter 10, Silva-Navarro et al. present the design of a passive/active autoparametric pendulum-type absorber to control the resonant vibrations in damped Duffing systems. Some simulation results are included in the chapter in order to illustrate the dynamic performance of the proposed system.

Part II contains 3 chapters related to solid-state materials and electron devices:

Chapter 11, by Juárez-Díaz et al., studies the effect of postgrowth thermal annealing processes on the optical characteristics of the zinc oxide (ZnO) films grown on (001) silicon substrates by DC reactive magnetron sputtering. The main motivation

for this work was to enhance the PL response and to identify the origin of deep-level luminescence bands. Results indicate that the ZnO films annealing have potential applications in optoelectronic devices.

Albarrán et al. present in chapter 12 a description of the spinodal decomposition of the $GaSb_xN_yAs_{1-x-y}$ quaternary alloys lattice-matched to the GaAs as the result of the internal deformation and coherency strain energies. The authors show ranges of spinodal decomposition of the $GaSb_xN_yAs_{1-x-y}$ alloys up to $y \leq 0.035$ with and without coherency strain energy.

Finally, in chapter 13, Morales-Sánchez et al. investigate the properties of amorphous and fcc polycrystalline $Ge_2Sb_2Te_5$ phases as well as the crystallization kinetics. The authors indicate that the various resistance states reached by annealing at different temperatures, suggest the possibility of using the $Ge_2Sb_2Te_5$ material as the active layer in a multi-state memory device.

Part III contains the following 7 chapters related to biomedical engineering, circuits and communication systems:

Vera et al., present in chapter 14, a study that compares four time-delay estimation methods, which relate temperature changes inside tissue replica (phantom) with time shifts in ultrasound echo-signals. The simulated signals were obtained from a numerical phantom which is proposed by the authors, and experimental signals were acquired from a specially developed agar phantom with uniformly distributed scatterers.

Chapter 15, by Ramírez-Mireles and Almada, presents a method for assessing the statistical nature of the multiple-access interference in wireless sensor networks. The authors propose a low-complexity method to establish “Gaussianity regions” in a two dimensional plane and determine the boundary of such regions for three different conditions: an ideal propagation channel with perfect and imperfect power control, as well as a multipath channel with “perfect average” power control.

In chapter 16, Cortez et al. present a family of hybrid codes, known as *LD STBC-VBLAST* codes, along with a receiver architecture suitable for low-complexity hardware implementation. The authors also present a correlated MIMO channel model and explore the impact of correlation on code performance. They show that *LD STBC-VBLAST* codes exhibit higher performance than other (recently-proposed) hybrid codes.

Lozano et al. present in chapter 17 a numerical integration considering shadowed and illuminated currents in physical optics in order to calculate the radiation pattern of antennas on complex structures modeled by NURBS. This approach is adopted for the case in which the antenna is placed at a distance less than one wavelength of the structure. The results are compared to measurements obtained with other physi-

cal optics techniques, such as the stationary phase method or numerical integration considering only illuminated currents.

Medina-Vázquez et al. show in chapter 18, the differences and advantages that the multi-input floating gate MOS (MIFGMOS) transistor has versus the conventional CMOS transistor. In order to illustrate such differences, the authors design and implement both a voltage to current converter cell and a memory current cell using MIFGMOS transistors. The development is based in mathematical and simulation analysis as well as in experimental results.

In chapter 19, Aguirre-Hernandez and Linares-Aranda present an $8\times8$-bits CMOS pipelined multiplier built using a full-adder cell with a new internal logic structure and a pass-transistor logic style that allow to get reduced delay and power consumption. A test chip containing the multiplier was fabricated using a $0.35\mu$m CMOS technology. The authors could confirm, through experimental measurements, its operation at 1.2GHz with a power consumption of 180mW, for a supply voltage of 3.3V.

Finally, chapter 20, by Medina Hernández et al., presents a new model for the production of autowaves which is used for navigation control of a mobile robot. Necessary analytic conditions based on linear theory are established in such a way that a reaction-diffusion system has an oscillating behavior in the initial phase.

Part IV contains the following 8 chapters related to computer science and computer engineering:

Chapter 21, by Cazarez-Castro et al., introduces a type-2 fuzzy logic controller whose intended task is to achieve the output regulation of a servomechanism with backlash. The design of this controller is optimized by a genetic algorithm aiming to obtain the closed-loop system in which the load of the driver is regulated to a desired position.

In chapter 22, Ferretti et al. presents what aims to be a general approach to combine autonomous robot navigation with high-level reasoning. In their proposal, they integrate vision-based motion planning with defeasible decision making (using logic programming) for differential-wheeled robots.

Galán Hernández and León Chávez present, in chapter 23, an object-oriented model of an open source software e-learning platform called Moodle. The model was developed using the Unified Model Language, and includes an analysis of its security services and vulnerabilities.

In chapter 24, Algredo-Badillo et al., provide a study in which they show how the software radio paradigm can be used to implement in hardware several standard security architectures within a single flexible platform.

Chapter 25, by de la Fraga, presents a method to efficiently build a mesh of triangles from a contour map of a terrain. The proposed approach includes intermediate points among contour lines to avoid the problem of flat triangles. The intermediate points are selected from the skeleton of the contour lines, and their heights are calculated automatically.

Barilla and Spann present in chapter 26 an experimental analysis of color-based texture image classification in order to evaluate whether or not the color and texture information should be used jointly or separately. Their results show that, indeed, color and texture information should be treated separately.

In chapter 27, López-García et al. report a software performance comparison of ten blind signature schemes that have been proposed between 1983 until 2008. The chapter provides a brief introduction to the basic concepts of blind digital signatures, and then provides an algorithmic description of the ten schemes studied along with the corresponding main arithmetic building blocks.

Finally, in chapter 28, Hernández León et al. propose a new algorithm for mining frequent itemsets. The proposed approach compresses the data while maintaining the necessary semantics for the frequent itemsets. This algorithm was found to be more efficient than other approaches that use traditional compression algorithms.

We we wish to thank all the authors for their high-quality contributions to this volume.

Finally, we wish to express our appreciation to LOGOS Verlag for their accomplished handling of the manuscript, for their understanding and for their patience.

*Carlos A. Coello Coello*
*Alexander Poznyak*
*José Antonio Moreno Cadenas*
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# 18

# Analisys of both a Voltage-to-Current Converter and a Memory Cell Implemented using the Multiple-Input Floating Gate MOSFET Transistor

A. Medina-Vázquez[1], J. Moreno-Cadenas[1], F. Gómez-Castañeda[1], Luis Martín-Flores[1], and M. E. Meda-Campaña[2]

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**Summary.** Differences and advantages that the Multi-Input Floating Gate MOS (MIFGMOS) transistor has versus the conventional CMOS transistor are shown. In order to do this, the design and implementation of both a Voltage to Current Converter (VIC) cell and a Memory Current Cell (MIC) using MIFGMOS transistors is presented. The development is based in mathematical and simulation analysis as well as in experimental results. Both cells present good performance and linearity according to theoretical analysis and presents low voltage operation and low power consumption, despite the long channel technology. These characteristics are very important in analog and mixed signal applications, like mobile communications systems. The cells presented here can be part of a low-voltage sample and hold circuit but applications are not restricted. Additionally, some comparison between simulation and experimental results obtained when testing five 3-input MIFGMOS transistor are included in order to show the properties and behavior of this transistor.

## 18.1 Introduction: Multiple-Input Floating Gate MOSFET Transistor

The floating gate MOSFET (FGMOS) transistor is a simple MOSFET transistor with its gate completely insolated, that means, without metal contact to the outside. The gate is immersed in an oxide layer and the electric charge into the floating gate does not flow to either side. For this reason, the floating gate transistor was used in implementing EPROM or EEPROM memories some decades ago [1], because the electric charge remain in the floating gate for a long time. However, currently it is possible to implement a great variety of analog and digital circuits based in FGMOS transistors [2] and [3], respectively. These kinds of circuits can be applied in communications systems as shown in [4], neural network [5], biomedical systems, etc. In general, in all these applications, low supply voltage and low power consumption are desired.

Because the gate of the MOSFET in a FGMOS is floating, it is necessary implement some mechanism to manipulate the electric charge or voltage on the

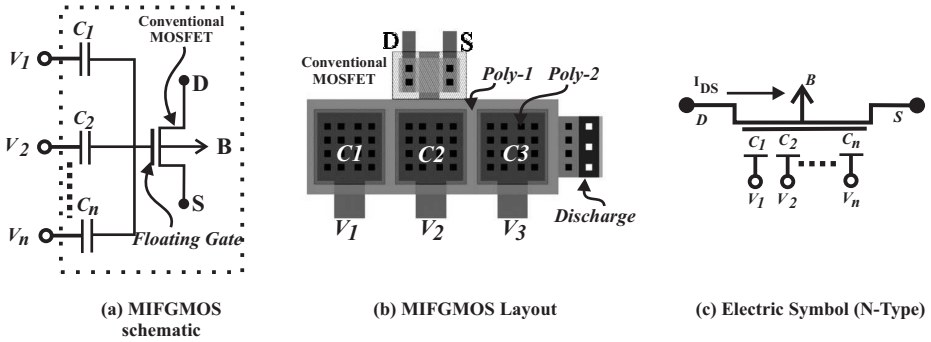


**Fig. 18.1.** Basic MIFGMOS transistor structure: (a) schematic, (b) 3-input MIFGMOS layout, (c) electric symbol

floating gate. The most popular techniques are: using ultraviolet light [6], Fowler-Nordheim tunneling [7], hot electron injection [8], quasi-floating gate [9], and capacitive coupling [10]. The approach presented here is focused to using the capacitive coupling in order to control the voltage on the floating gate. It is necessary to note that using this technique, multiple inputs are possible.

As shown in Fig. 18.1(a), Multi-input Floating Gate MOS (MIFGMOS) transistor has many input gates ($V_1$, $V_2$,..., $V_n$) coupled to the gate of a conventional MOSFET trough capacitors ($C_1$, $C_2$,..., $C_n$). Fig. 18.1(b) shows the layout of a three-input MIFGMOS and part (c) shows the electrical symbol.

The coupling capacitors are formed by the poly1 layer (the floating gate) and poly2 layer. It is recommendable to use poly1-poly2 capacitors because the gate is always built with poly1 layer and furthermore, there is more capacitance per unit area than using metal1-metal2 capacitors. Hence, input voltages ($V_1$, $V_2$,..., $V_n$) are coupled through the capacitors to the floating gate to modify the drain-source current [10]. In this manner, the input voltages can be coupled and added arithmetically to the floating gate. This is because the floating gate voltage is a function of the input voltages $V_i$ and the coupling capacitors $C_i$. In general, the input voltages $V_i$ are called control inputs. Thus, the floating gate voltage can be approximated by [11]:

$$V_{FG} = \sum_{i=1}^{n} \frac{C_i}{C_T} V_i + \frac{C_{FGS}}{C_T} V_S + \frac{C_{FGD}}{C_T} V_D + \frac{Q_{FG}}{C_T} \tag{18.1}$$

where $n$ is the number of inputs coupled capacitively, $C_i$ are the coupling capacitances, $V_i$ are the input voltages, $V_S$ and $V_D$ are the source and drain voltages, respectively, $Q_{FG}$ is the initial charge in the floating gate, and $C_T$ is given by:

$$C_T = \sum_{i=1}^{n} C_i + C_{FGD} + C_{FGS} \tag{18.2}$$

In (18.2), $C_{FGD}$ and $C_{FGS}$ are the floating-gate-drain and floating-gate-source parasitic capacitances, respectively.

In this way, the first approximation equation to determine the drain-source current in sub-threshold regime, triode and saturation region are, respectively:

$$I_{DS} = I_{DO}\frac{W}{L}\exp\left(\frac{V_{FGS}-V_{th}}{\eta V_{ther}}\right) \text{ if } V_{FGS} < V_{th} \text{ and } V_{DS} < 4V_{ther} \tag{18.3}$$

where $V_{ther}$ is the thermal voltage approximated by $\frac{kT}{q}$ (k is the Bolztman constant, T is temperature and q the electron electric charge). $I_{DO}$ is a drain-source current when $V_{FGS} = V_{th}$ and $\eta$ is a constant, usually 1, and $V_{th}$ is the MOSFET threshold voltage.

$$I_{DS} = K'\frac{W}{L}\left((V_{FGS}-V_{th}) - \frac{V_{DS}}{2}\right)V_{DS} \text{ if } 0 < V_{DS} < (V_{FGS}-V_{th}) \tag{18.4}$$

where $K' = \mu_o C_{ox}$ and $W/L$ is the MOSFET geometry

$$I_{DS} = K'\frac{W}{L}(V_{FGS}-V_{th})^2 \text{ if } 0 < (V_{FGS}-V_{th}) < V_{DS} \tag{18.5}$$

In (18.3)-(18.5) $V_{FGS}$ is approximated by (18.1).

On the other hand, an important consideration is the unpredictable charge stored in the floating gate when the MIFGMOS transistor is fabricated. This charge remain on the floating gate for a long time, so it can changes the circuit performance. To solve this problem, the technique presented in [12] is used here, where the undesirable electrical charge is removed during the manufacturing process using switchs formed by metal contacts.Other methods to discharge the initial charge in the floating gate (do not used here) are: ulraviolest light, Fowler-Nordheim technique and quasi-floating gate technique, all referenced above.

### 18.1.1 Simulation and d.c. results

To get the current-voltage simulation of the MIFGMOS transistor and compare it with the experimental results, some simulations models published in the literature were considered [13], [14], [15]. All this models have positive and negative characteristics and the search for better models continues. However, the model presented in [15] was considered in this work, because it calculates the floating gate voltage based in the parameters provided for the manufacturer and its SPICE implementation is simpler. Then, to compare the d.c. simulation results with the experimental results, five 3-input MIFGMOS coupled inputs were fabricated in $1.2\mu$m technology. Table 18.1 shows the values of the coupling capacitances and ratio aspect as well other important parameters of each MIFGMOS transistors after they were fabricated. Additionally, Table 18.2 shows the capacitive parameters of the $1.2\mu$m process.

Thus, the three inputs $V_{G1} = V_{G2} = V_{G2}$ of the MIFGMOS represented in Fig. 18.2 are connected toghether and they has been sweep while $V_{DD}$ is kept constant. In Fig. 18.3, the experimental average results (measuring the experimental median results of five transistors) are ploted when $V_{DD} = 1.0V$ and $V_{DD} = 3.0V$, respectively. It is possible to see simulation results are according to experimental results.

**Table 18.1.** Coupling capacitances and ratio aspect of the 3-input MIFGMOS transistor

| Parameter | Value | Description |
|---|---|---|
| $C_1$ | 50.1984fF | Coupling capacitor 1 |
| $C_2$ | 40.9953 | Coupling capacitor 2 |
| $C_3$ | 96.6319 | Coupling capacitor 3 |
| $W_n$ | $6.0\mu$m | Channel wide |
| $L_n$ | $3.6\mu$m | Channel lenght |
| $\lambda$ | $1.2\mu m$ | CMOS process technology |
| $\mu_o$ | 647.91 $cm^2/Vs$ | Low-field Mobility (n-type) |
| $K'(\mu_o C_{ox})$ | $21.1\mu A/V^2$ | Transconductance parameter |
| $V_{th}$ | 0.59V | n-type MOSFET sub-threshold voltage |
| $t_{ox}$ | 316 Å | Gate-oxide thickness |

**Table 18.2.** Capacitance parameters in the $1.2\mu m$ CMOS process

| Parameter | N+ | P+ | Poly1 | Poly2 | Metal1 | Metal2 | Units |
|---|---|---|---|---|---|---|---|
| Area(sustrate) | 290 | 304 | 37 | 37 | 24 | 16 | aF/$\mu m^2$ |
| Area(N+ active) | - | - | 1094 | 696 | 52 | 27 | aF/$\mu m^2$ |
| Area(P+ active) | - | - | 1079 | 690 | - | - | aF/$\mu m^2$ |
| Area(Poly1) | - | - | - | 581 | 46 | 23 | aF/$\mu m^2$ |
| Area(Poly2) | - | - | - | - | 47 | 23 | aF/$\mu m^2$ |
| Area(metal1) | - | - | - | - | - | 38 | aF/$\mu m^2$ |
| Fringe(sustrate) | 73 | 157 | - | - | 30 | 26 | aF/$\mu$ m |
| Fringe(poly1) | - | - | - | - | 60 | 43 | aF/$\mu$ m |
| Fringe(metal1) | - | - | - | - | - | 55 | aF/$\mu$ m |
| Overlap(N+ active) | - | - | 256 | - | - | - | aF/$\mu$ m |
| Overlap(P+ active) | 256 | - | - | - | - | - | aF/$\mu$ m |

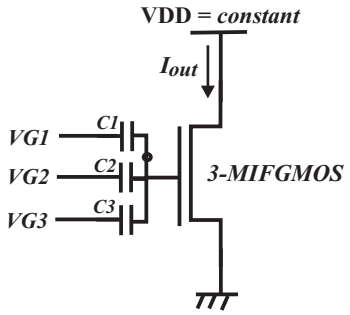


**Fig. 18.2.** Configuration to analyze d.c. curves of the 3-input-MIFGMOS

### 18.1.2 Programmable threshold voltage

As it was mentioned early, the MIFGMOS transistor has a tuning property because it can increase or decrease its relative threshold voltage dynamically using a single

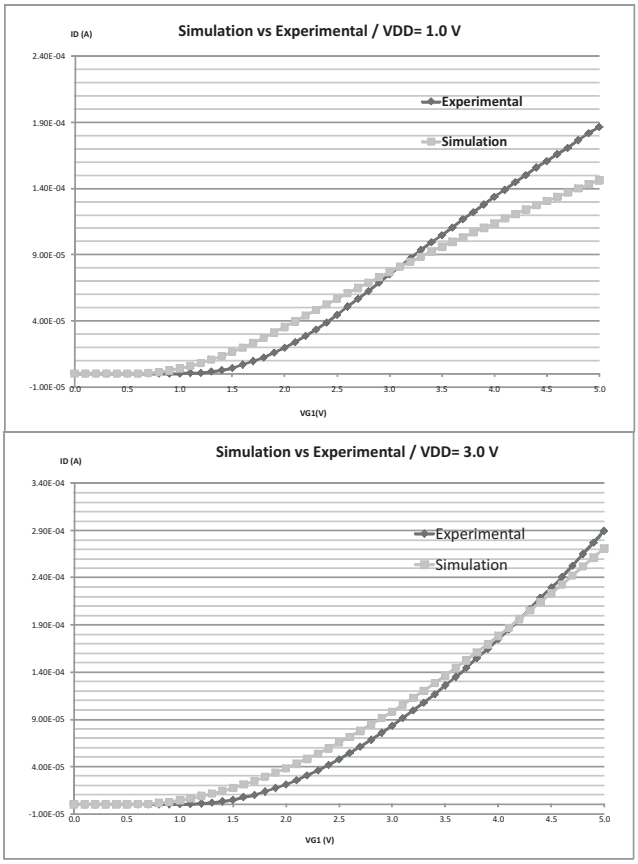


**Fig. 18.3.** Comparation between experimental and simulation $I_{DS}$ vs. $V_{G1}$ curves

coupled input gate. This can be interpreted as a programmable apparent threshold voltage. To show this, an experimental test is done setting the inputs of the transistor in Fig. 18.2 as follows: two inputs ($V_{G2}$ and $V_{G3}$) are connected together to apply a sweep input voltage, and the input $V_{G1}$ will be used to control the relative threshold voltage. The $V_{G1}$ voltages take values of -5.0, -3.0, -1.0, 0.0, +1.0, +3.0 and +5.0 volts. In this case, the supply voltage $V_{DD}$ is maintained constant with a value of 5.0V. Fig. 18.4 shows the $I_{DS}$ vs. $V_{G1}$ curves, where $I_{DS}$ is the drain current of the transistor. We can note a particular case when $V_{G1}$=+5.0V, there is a small current flowing in the transistor even if the input voltage $V_{G1}$ is zero. This could be a disadvantage in a circuit based on MIFGMOS transistor because is necessary to cut this current when the transistor is not required, using additional transistors as switches.

However, modifying the relative MIFGMOS threshold voltage, we can get positive consequence since the supply voltage and operation voltage can be reduced, e.g. in cascode configurations in a CMOS design, where to maintain the transistor working in the saturation region it is needed that each transistor satisfy $V_{DS} =$

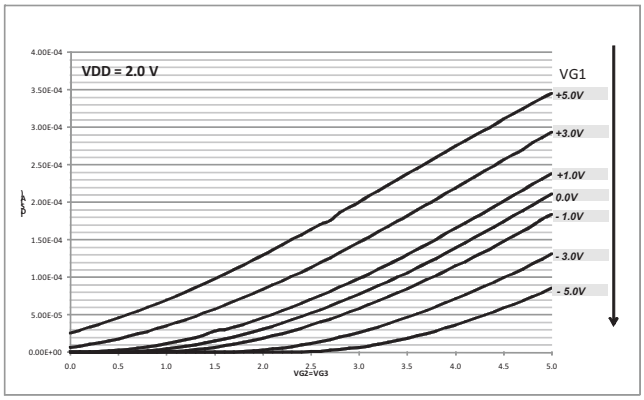


**Fig. 18.4.** Drain-source current of MIFGMOS transistor when the apparent threshold voltage is varied (experimental results).

$V_{GS} - V_{th}$, thus, if the threshold voltage $V_{th}$ or the gate-source voltage $V_{GS}$ can be manipulated, $V_{DS}$ can be reduced, [16] and [17] and, consequently, we can reduce the supply voltage $V_{DD}$. Moreover, decreasing the supply voltage, the total power dissipation of the circuit is decreased.

### 18.1.3 Other properties of the MIFGMOS

The MIFGMOS transistor has another propierty, that is, the possibility of a feedback loop to improve the linearity in a particular desing and this will be shown later. More even, using MIFGMOS transistors the circuit complexity is reduced, signal processing is simplified and the quiscient point in a circuit can be shifted [13]. All advantages mentioned above are very important both in analog and in mixed signal circuits design, particularly in applications which require low supply voltage and low power dissipation, as used in [18] and [19].

However, the MIFGMOS has some disadvantages when is compared with the conventional MOSFET. The most important disadvantages are: lower effective transconductance, lower output resistance, and lower frequency response. If we define the effective MIFGMOS transconductance (in saturation region) respect to a single input $V_i$ as

$$g_{mi} = \frac{\delta I_{DS}}{\delta V_i} \tag{18.6}$$

from (18.5) and (18.6) we get the expression:

$$g_{mi} = \frac{\delta I_{DS}}{\delta V_i} = \frac{\delta}{\delta V_i}\left(\frac{1}{2}\mu_o C_{ox}\frac{W}{L}\left(\frac{C_i}{C_T}V_i + \sum_{x=2}^{n}\frac{C_x}{C_T}V_x - V_{th}\right)\right) \tag{18.7}$$

and

$$g_{mi} = \frac{C_i}{C_T} g_m \tag{18.8}$$

where $g_m$ is the transconductance of the conventional MOSFET transistor. Note than the transconductance of the MIFGMOS respect to a single input is lower than the conventional MOSFET ($\frac{C_i}{C_T} < 1$).

## 18.2 Voltage to current converter based on MIFGMOS

The Voltage-to-current converter (VIC) cell based on the MIFGMOS transistor is presented and analyzed here to show the properties of the MIFGMOS such as: low-power operation, good linearity at low voltage operation and configurable threshold voltage. The advantages mentioned above are very important both in analog and in mixed signal circuits design, particularly in applications which require low voltage operation and low power dissipation.

The main function of the VIC is to convert an input voltage to an output current. We are interested in a VIC designed with MIFGMOS transistors to take advantages about its properties mentioned above.

This cell consists of a linear transconductor and a p-type current mirror as a load, both implemented with MIFGMOS transistors, as shown in Fig. 18.5. In this cell M1 is the transconductor with M6 as a triode load. The p-type current mirror (M8-M11) operates as a load in order to reduce the channel-length modulation and improve the circuit gain. M1 transistor has a feedback loop between its drain and the floating gate through $C_f$ capacitance to improve the linearity of the cell. However, if the cell has a $V_{DDFG}$ voltage applied, it will be a voltage $V_f$ coupled to the floating gate through $C_f$, thus, we have a current IM6, even if $V_{in}$ is null. This could be an undesired effect. To cut this undesired current when the cell is not needed, we use the transistors M3, M5 and M7 as switches.

In the next subsection each part is analyzed and it is showed how the VIC cell proposed here requires less supply voltage maintaining good linearity than conventional MOSFET version.

### 18.2.1 Transconductor stage

Now, it is showed how the transconductor stage in the VIC in Fig. 18.5, proposed here, has better linearity than conventional MOSFET version.

Analyzing M1 transistor and based in (18.1), the floating gate voltage is calculated by:

$$V_{FG1} \approx \frac{C_{in} V_{in}}{C_T} \tag{18.9}$$

ignoring $C_{GD}$, $C_{GS}$, $C_{GB}$ and $C_{ox}$ effects in order to facilitate hand calculations without losing generality.

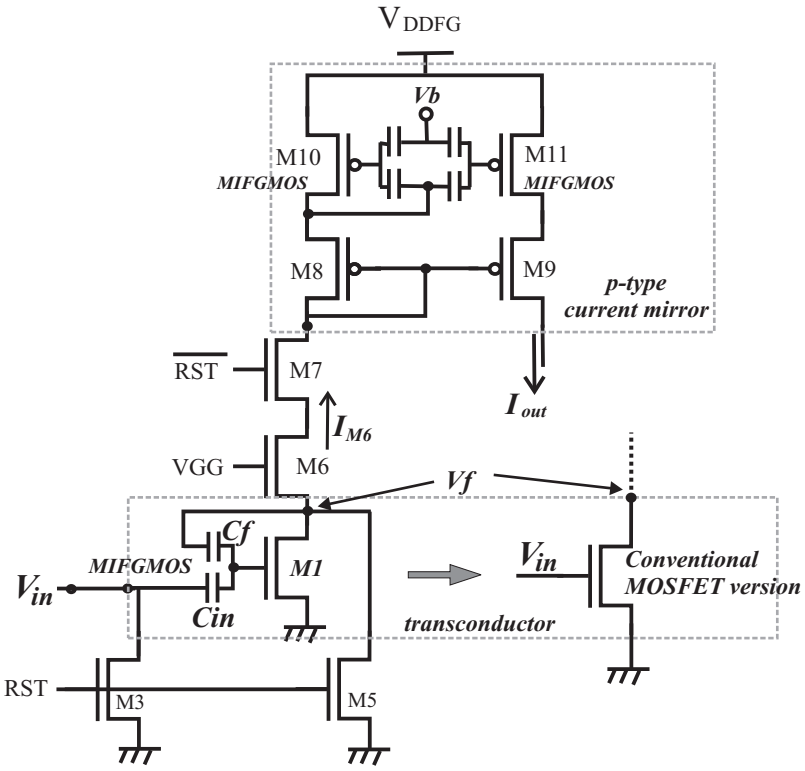


**Fig. 18.5.** Voltage to current converter implemented with MIFGMOS transistors. M1 MIFGMOS is compared with a conventional MOSFET

Taking M6 triode load, M7 switch, and p-type current mirror together shown in Fig. 18.5 as a load called $R_D$, the drain voltage $V_f$ of M1 in saturation region is:

$$V_f = V_{DDFG} - R_D \frac{\mu_o C_{ox}}{2} \frac{W_1}{L_1} \left( \frac{C_{in}}{C_T} V_{in} + \frac{C_f}{C_T} V_f - V_{th} \right)^2 \tag{18.10}$$

where $\mu_o$ is the mobility of charge carriers, $C_{ox}$ is the MOSFET gate oxide capacitance by unit area, $V_{th}$ is the threshold voltage for n-type MOSFET, and $L$ and $W$ are the large and width of the MOSFET transistor, respectively.

Developing the squared term in (10), we get:

$$\begin{aligned} V_f = V_{DDFG} - R_D \frac{\mu_o C_{ox}}{2} \frac{W_1}{L_1} (V_{th}^2 - \frac{2C_{in}}{C_T} V_{in} V_{th} - \frac{2C_f}{C_T} V_f V_{th} \\ + \frac{2C_{in} C_f}{C_T^2} V_f V_{in} + \frac{C_{in}^2}{C_T^2} V_{in}^2 + \frac{C_f^2}{C_T^2} V_f^2) \end{aligned} \tag{18.11}$$

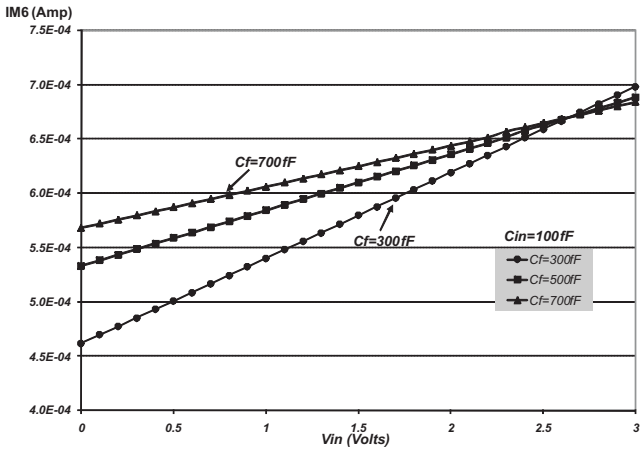


**Fig. 18.6.** $I_{out}$ vs. $V_{in}$ in MIFGMOS transconductor (simulation)

In (18.11) there are three squared terms. In this case, $V_{th}$ is constant ($\approx 0.7$V, according to the $1.2\mu m$ technology), but we can have control in the two last terms: $\frac{C_{in}^2}{C_T^2}V_{in}^2$ and $\frac{C_f^2}{C_T^2}V_f^2$.

So, linearity improves increasing $C_T$ since $(C_T = C_{in} + C_f)$, it means, it is necessary to increase $C_{in}$ or $C_f$. We opted arbitrary to increase the value of $C_f$ to increase $C_T$. It should be noted this property is not possible using conventional MOSFET transistor.

Fig. 18.6 shows the IM6 current (drain of M6 transistor), when the input voltage of the VIC ($V_{in}$) is swept, also, $C_f$ is varied. Note the good linearity with 2.0V voltage supply ($V_{DDFG}$) using a resistor as a load ($R_D = 10k\Omega$) . Also, note that the output current IM6 is different to zero when $V_{in} = 0V$. This is because the feedback voltage $V_f$ is present when $V_{DDFG}$ is applied. This current means static power consumption but it can be cut using the switches mentioned above. Here, $C_{in} = 100\,fF$.

Fig. 18.7 shows a simulated comparison between the drain current flowing through M1 transistor working as the transconductor shown in Fig. 18.5, both MOSFET and MIFGMOS version. In these cases, the supply voltage is 3.0V. We can see better linearity in MIFGMOS version but better dynamic range (RD) in MOSFET case.

### 18.2.2 Low-supply voltage p-type current mirror

Now, it is showed how the p-type current mirror proposed and implemented with MIFGMOS transistors (Fig. 18.8(a)) will require less supply voltage than conventional MOSFET version (Fig. 18.8(b)). So, we demonstrate that:

$$V_{DDC} > V_{DDFG} \tag{18.12}$$

Each version is analyzed and compared.

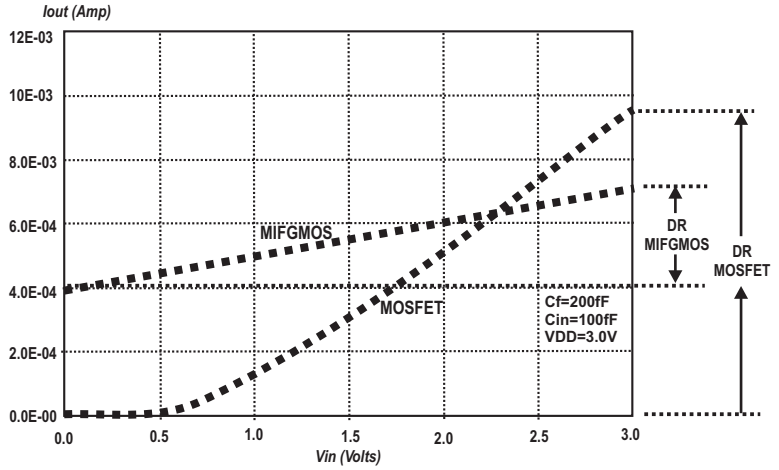


**Fig. 18.7.** Comparison between MIFGMOS and conventional MOSFET transconductor (simulation)

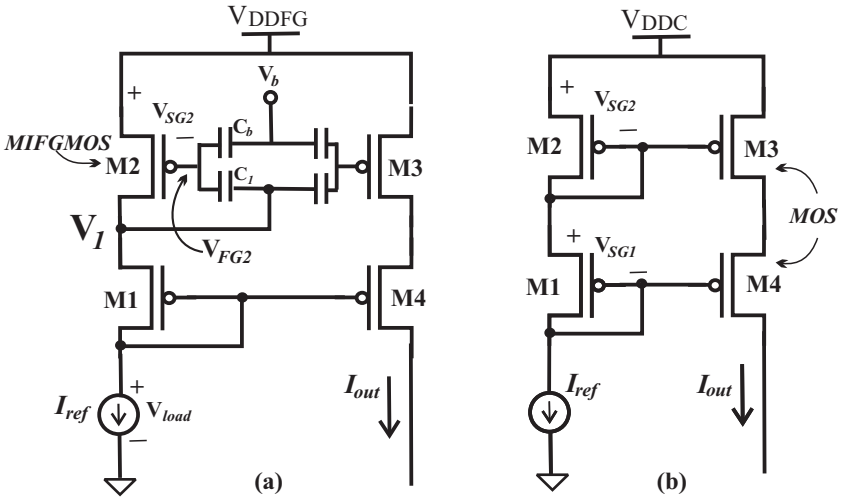


**Fig. 18.8.** (a) P-type current mirror implemented with MIFGMOS transistor and (b) implemented with MOSFET transistors only

### a. Current mirror implemented using conventional MOSFET transistors only

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Analyzing the circuit showed in Fig. 18.8(b), the supply voltage $V_{DDC}$ is:

$$V_{DDC} = V_{GS2} + V_{GS1} + V_{load} \tag{18.13}$$

where $V_{load}$ is the voltage provided for the current source $I_{ref}$ . In this case, we consider all the transistors working in the saturation region, hence the source to gate voltage of M1 or M2 is:

$$V_{SG1} = \sqrt{\frac{2I_{ref}}{\mu_o C_{ox}} \cdot \frac{L_1}{W_1}} + V_{thp} \tag{18.14}$$

where $V_{thp}$ is the threshold voltage for p-type MOSFET transistor.

Now, combining (13) and (14) we obtain:

$$V_{DDC} = 2V_{thp} + \sqrt{\frac{2I_{ref}}{\mu_o C_{ox}}} \left( \sqrt{\frac{L_2}{W_2}} + \sqrt{\frac{L_1}{W_1}} \right) + V_{load} \tag{18.15}$$

The result obtained in (18.15) is very important because it shows the way the supply voltage depends of $V_{load}$ and both the aspect ratio and $V_{thp}$. Also, we will use (18.15) to demonstrate (18.12).

**b. Current mirror implemented using the conventional MOSFET transistor**

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Similar analysis is realized for the current mirror MIFGMOS version. In Fig. 8(a), the current through M2 transistor in saturation region is:

$$I_{ref} = \frac{\mu_o C_{ox}}{2} \frac{W_2}{L_2} \left( V_{DDFG} - V_{FG2} - V_{thp} \right)^2 \tag{18.16}$$

where the floating gate voltage of M2 ($V_{FG2}$) is given by:

$$V_{FG2} = \frac{C_1 V_1 + C_b V_b}{C_T} \tag{18.17}$$

In (18.17), $V_b$ is a small bias voltage applied to the p-type MIFGMOS transistors in order to decrease the relative threshold voltage of M2 and consequently to reduce the supply voltage ($V_{DDFG}$). $C_1$ and $C_b$ are coupling capacitors. Later, ignoring the parasitic capacitances $C_{GD}$, $C_{GS}$, and $C_{GB}$ and combining (18.16) and (18.17), the supply voltage is:

$$V_{DDFG} = \sqrt{\frac{2I_{ref}}{\mu_o C_{ox}} \frac{L_2}{W_2}} + \frac{C_b}{C_T} V_b + \frac{C_1}{C_T} V_1 + V_{thp} \tag{18.18}$$

where the voltage in node $V_1$ is given by:

$$V_1 = V_{SG1} + V_{load} \tag{18.19}$$

Finally, combining (18.14), (18.18), (18.19):

$$V_{DDFG} = V_{thp} + \frac{C_1}{C_T} V_{thp} + \frac{C_b}{C_T} V_{load} + \sqrt{\frac{2I_{ref}}{\mu_o C_{ox}}} \left( \sqrt{\frac{L_2}{W_2}} + \frac{C_1}{C_T} \sqrt{\frac{L_1}{W_1}} \right) \tag{18.20}$$

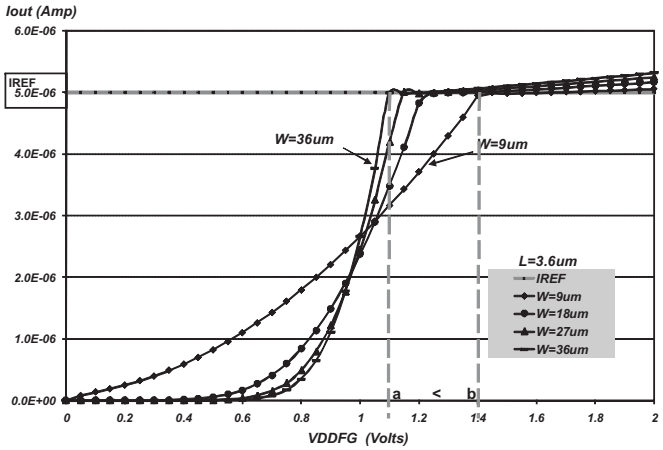


**Fig. 18.9.** $I_{out}$ vs. $V_{DDFG}$ for different geometries (simulation)

Equation (18.20) calculates the minimum supply voltage needed for the current mirror transistors working in the saturation region. Fig. 18.9 shows the curves of $V_{DDFG}$ voltage versus $I_{out}$. In this case, a current of $5\mu A$ is applied as a target and $C_1 = C_b = 100\,fF$.

It is possible to watch that modifying the ratio aspect of the transistor the supply voltages $V_{DDFG}$ ca be reduced. This is shown in the simulation results in Fig. 18.9 for different values of $W$, maintaining $L = 3.6\mu m$. When $W$ is increased, less supply voltage $V_{DDFG}$ is required to copy the target current maintaining the transistors in saturation region (see points *a* and *b*). However, a tradeoff exists between low supply voltage and linearity and this must be taken into account in the design process.

In order to analyze the effect of the bias voltage $V_b$ in the current mirror in Fig. 18.8(a), Fig. 18.10 shows the current mirror operation varying $V_b$. We can see that applying a very small or negative voltage on $V_b$, the supply voltage $V_{DDFG}$ is reduced maintaining the transistor in the saturation region (see points *c* and *d*). In this case, $I_{ref} = 5\mu A$ and $C_1 = C_b = 100\,fF$.

Now, it is demonstrated than (18.12) is true. First, note that $V_{DDC}$ in (18.15) and $V_{DDFG}$ in (18.20) are always positive. Then subtracting (18.20) and (18.15), we have:

$$V_{DDC} - V_{DDFG} = V_{load}\left(1 - \frac{C_1}{C_T}\right) + V_T\left(1 - \frac{C_1}{C_T}\right) + \sqrt{\frac{2I_{ref}}{\mu_o C_{ox}}\frac{L_1}{W_1}}\left(1 - \frac{C_1}{C_T}\right) + \frac{C_b}{C_T}V_b \tag{18.21}$$

Since $0 < C_1 < C_T$:

$$0 < (1 - \frac{C_1}{C_T}) < 1 \tag{18.22}$$

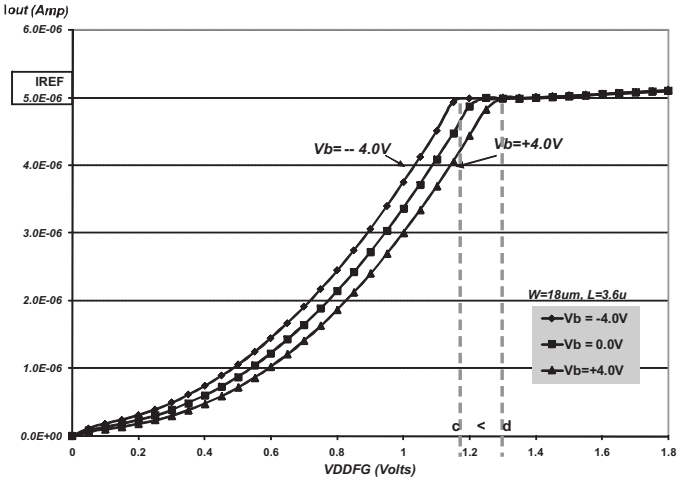


**Fig. 18.10.** $V_b$ impact in the p-type curent mirror. $I_{out}$ vs. $V_{DDFG}$ changing $V_b$ (simulation)

Hence, all terms in (18.21) are always positives ($V_b$ could be zero), so we conclude that $V_{DDC} > V_{DDFG}$.

## 18.3 VIC implementation

The VIC cell was fabricated in a $1.2\mu m$ CMOS technology, double poly, double metal. Fig. 18.11 shows the experimental results when we measured the linearity of the VIC. To do this, an input voltage is swept in $V_{in}$ input and the output current $I_{out}$ is measured. Note the good linearity of this cell with a voltage supply of 1.7V.

Fig. 18.12 (scope image) shows the operation of the VIC cell when is used as a code detector in a signal processing. In this case, $V_{in}$ is a binary sequence "10011100", with amplitude of $0V$ to $500mV$ at $500kHz$ and a supply voltage $V_{DDFG}$ of $1.7V$. For reason of easy, the output voltage was measure using a $1.0k\Omega$ resistive load between the drain of M9 transistor and ground, which it has a maximum value of $8.0mV$. Now, the maximum output current of the VIC will be $8mV/1.0K\Omega = 8\mu A$. Meanwhile, if this cell operates with a higher supply voltage of $3.0V$, a speed operation of $2.0MHz$ is possible; but, it must take into account the load (discrete resistor of $1.0k\Omega$) in the drain of M9 used in the experimental measures because it will be a limiting factor. As we can see, this cell has a limited speed operation, thus, it is necessary to consider this characteristic in the design process.

## 18.4 Memory current cell (MIC)

In this section, a current memory cell implemented using MIFGMOS transistor is introduced. This cell is formed by n-type transistors current mirror. In previous

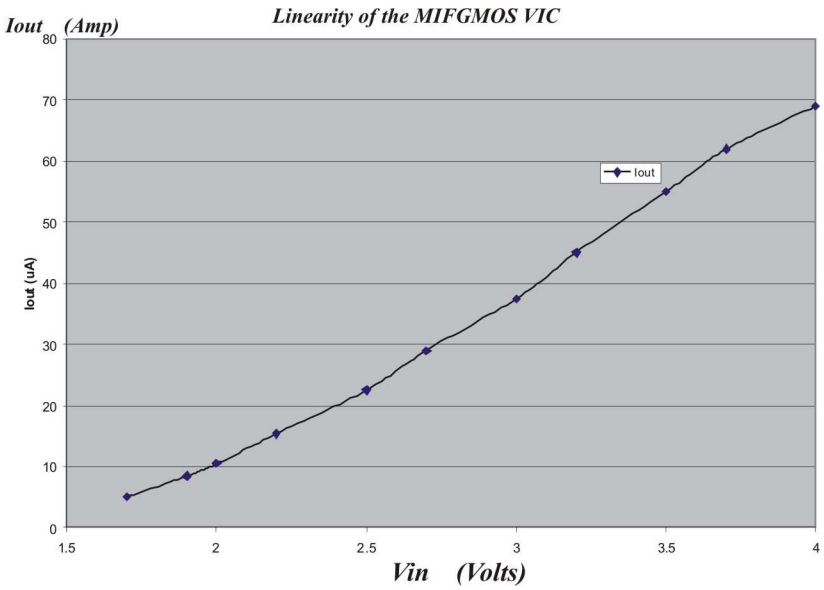


**Fig. 18.11.** linearity of the MIFGMOS VIC (experimental results)

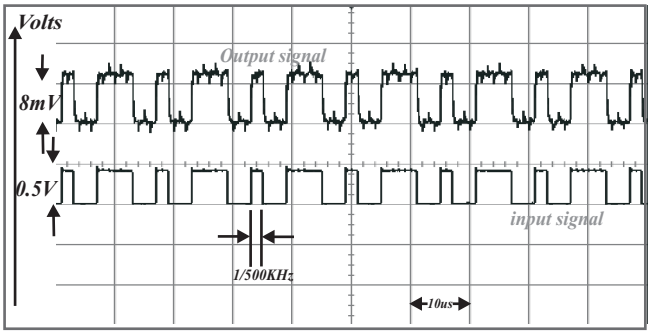


**Fig. 18.12.** Operation of the VIC at 1.7 V supply voltage (experimental result).

section the low-voltage operation of the current mirror implemented with MIFGMOS transistor was shown. Thus, the memory current cell shown in Fig. 18.13 stores an analog current as a charge and, connecting both the VIC and MIC cells in a cascade array, a low-voltage sample and hold circuit in current mode can be implemented.

The MIC implemented with MOSFET transistor is shown in Fig. 18.13(a) and the MIFGMOS version proposed here is shown in Fig. 18.13(b). The MIFGMOS MIC is a current mirror (M2, M4 and M5) used as a memory, where M1, M3 and M6 operate as switches.

This cell operates as follows: when M1 and M3 switches are closed and the M6 switch is opened, $I_{in}$ generates a voltage in the gate of M4. Later, cutting M1

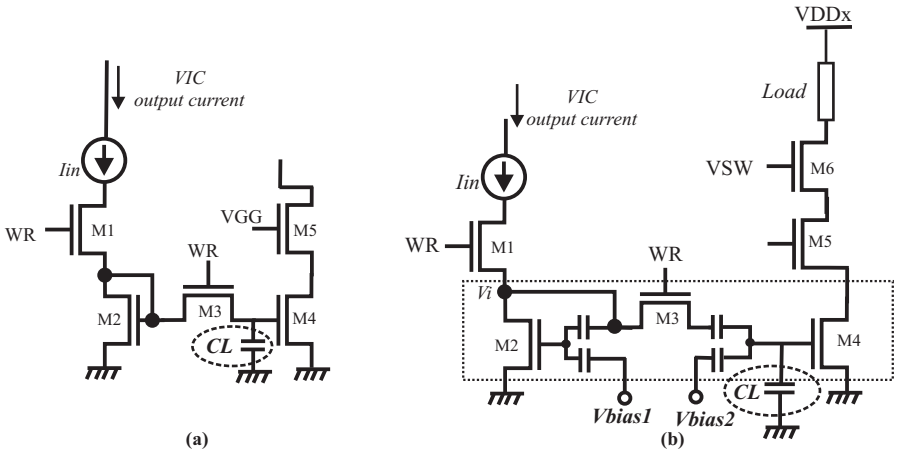


**Fig. 18.13.** Memory Current Cell (a) conventional MOS, (b) MIFGMOS version

and M3, a charge is stored in the gate-source parasitic capacitance ($C_L$) inherent to the MIFGMOS transistor M4. This stored charge will be proportional to the $I_{in}$ amplitude, representing the memory. When the M6 is closed, the voltage stored in $C_L$ will generate a current through M4, M5 and M6. In this case, the bias voltages $V_{bias1}$ and $V_{bias2}$ decrease the relative threshold voltage to get a minimal supply voltage in cascode configuration.

The MIC implemented with MIFGMOS transistors will have a better linearity with a minimal supply voltage $V_{DDx}$ because transistors M4-M6 are working in saturation region with less voltage thanks to the applied bias voltages to the floating gate. Thus, we take advantages from the properties of the MIFGMOS transistor to build a low-voltage MIC with a good linearity.

### 18.4.1 MIC implementation

The MIC shown in Fig. 18.12(b) using MIFGMOS transistors was implemented in a1.2$\mu m$ CMOS technology, double poly, double metal. In order to see the linearity of this cell, Fig. 18.15 shows a swept input current $I_{in}$ versus the output current through the transistors M4-M6 of the MIC. Here, the current is reduced intentionally with a rate of 3:1. The output current was measured between the drain of M6 and $V_{DDX}$ voltage.

Finally, Fig. 18.17 shows the operation of the MIC with a supply voltage $V_{DDx}$ of 1.7V (scope image). In this case, a low frequency sinusoidal signal of 500Hz is sampled using a 500 kHz sampling pulsed signal (0-3V). For reason of easy, the output is read in voltage mode using a $R_D$ load of 220$K\Omega$ to get an observable signal. Again, the speed of the cell is limited for high frequency applications because the high value of the resistor and the RC constant involved in all the measuring process. In order to enhance the bandwidth of the cell, a more elaborate I/V converter

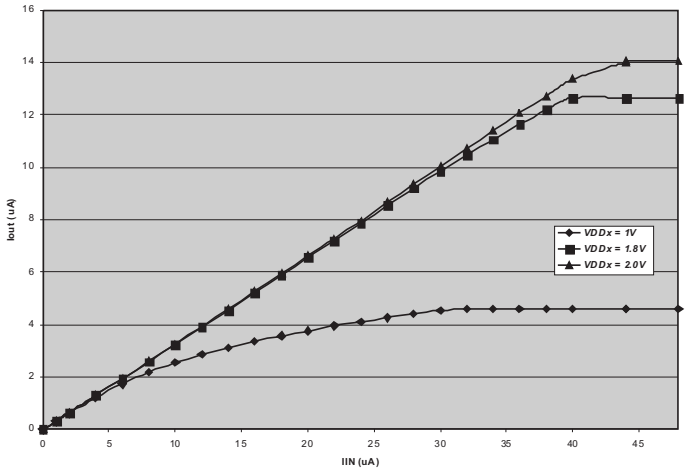


**Fig. 18.14.** Linearity of the MIFGMOS MIC. Iin vs. Iout. (experimental results)

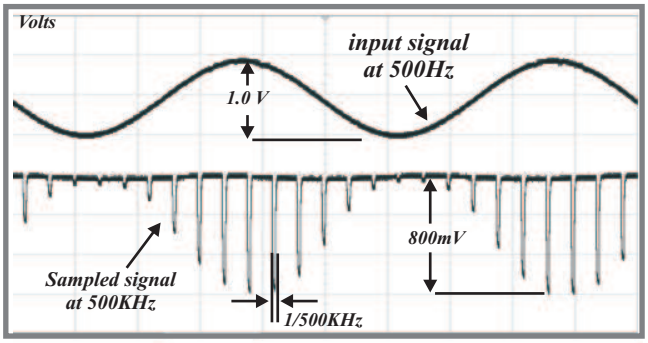


**Fig. 18.15.** Operation of the MIC with a voltage supply of 1.7V (experimental result).

is recommended. However, both cells are recommended for current mode circuit design.

## 18.5 Conclusions

This document shows than MIFGMOS transistor is an important alternative to implement analog circuits with low voltage operation and good linearity based in the advantages of this transistor. To demonstrate this, the analysis and implementation of two cells using MIFGMOS transistors were presented: a voltage to current converter cell and a memory current cell. Two important properties of MIFGMOS transistors

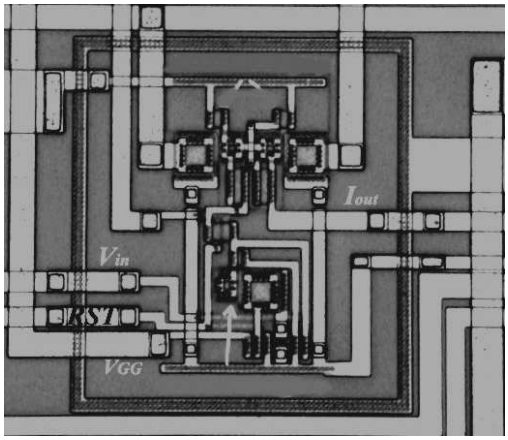


**Fig. 18.16.** MIcrofotography of the VIC

were shown: variable threshold voltage and feedback possibility. Combining these properties, a voltage to current converter with good linearity at low supply voltage was implemented. We compare the performance of the VIC in a MOSFET version versus a MIFGMOS version and we demonstrated with analytical and experimental results than MIFGMOS has a better linearity applying a low supply voltage, but with a low frequency operation. This must be taken into account in the process design.

On the other hand, a MIC using the MIFGMOS transistor was implemented in order to obtain good linearity with low supply voltage. We got satisfactory results despite the long-channel technology.

Both cells were implemented in a $1.2\mu m$ CMOS technology, double poly, double metal. The VIC operates satisfactory with 1.7V supply voltage at 0.5MHz with a power consumption of $20\mu W$. Also, the MIC can operate with a supply voltage of 1.7V with $12\mu W$ power consumption at 0.5MHz.

Finally, these cells can be used to implement a sample and hold circuit operating in current mode, but theirs applications are not limited. Fig. 18.16 and 18.17 show the micropotography of the VICand the MIC, respectively.

**Acknowledgment**

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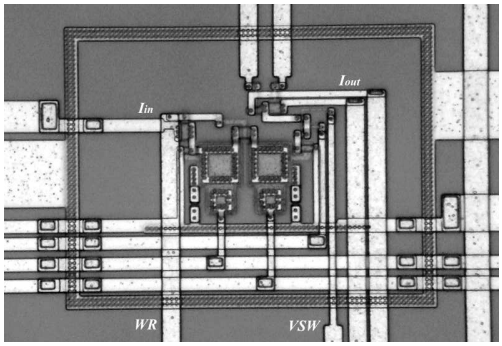


**Fig. 18.17.** MIcrofotography of the MIC

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