2012 9th International Conference on Electrical Engineering, Computing Science and Automatic Control
Mexico City, Mexico. September 26-28, 2012

4-Bit Arithmetic Logic Unit (ALU) based on Neuron MOS Transistors.

E. A. Cortés-Barrón[1], M. A. Reyes-Barranca [1], L. M. Flores-Nava[1], A. Medina-Santiago[2]
[1]Electrical Engineering Department, Solid State Electronics Section, CINVESTAV-IPN, Mexico D.F., México.
[2]Instituto Tecnológico de Tuxtla Gutiérrez, Chiapas, México
Phone (55) 5747 3776 Fax: (55) 5747 3978 E-mail: ecortes@cinvestav.mx, mreyes@cinvestav.mx, lmflores@cinvestav.mx, medinas23@yahoo.com.mx

Abstract —A **methodology is proposed for the design of a 4-Bit Arithmetic Logic Unit (ALU) based on Soft-Hardware-Logic (SHL). The core of the implementation is based on the device known as neu-MOS (ν-MOS), a floating-gate MOS transistor with more than one control gate used for the digital signal processing. This configuration is reconfigurable modifying only the external voltages applied to an intermediate stage of programmable CMOS inverters, without any circuitry change, in contrast with conventional digital implementations. Here it is demonstrated that using a universal circuit, basic Boolean functions like AND, NAND, OR, NOR, Exclusive-OR and Exclusive-NOR can be configured using Multiple-Input Floating-Gate (MIFG) Transistors or neu-MOS. Based on a graphical method called Floating-gate Potential Diagram (FPD), a very basic 4-Bit ALU was designed and simulated for a couple of arithmetic and logic functions taking advantage of the weighted sum performed at the floating gate of the neu-MOS. Weighted inputs can be obtained from the FPD and then converted to effective capacitances choosing a given CMOS technology, OnSemi's 0.5 μm technology, for instance. Results obtained from simulations of the proposed design are compared with experimental results of ALUs configured with a FPGA evaluation kit and Motorola's MC14581B ALU chip.**

Keywords — **Soft-Hardware-Logic, neu-MOS, ALU**

I. INTRODUCTION

The Multiple-input Floating-gate (MIFG) MOSFET, such as the neu-MOS Transistor (neuron-MOS), has multiple input gates and an electrically isolated floating gate which is capacitively coupled to input gates. It performs like a biological neuron where several signals arrive to a neuron, where they are processed to give an output depending on an activation function. Correspondingly, in a neu-MOS a weighted sum of the voltage applied to each of the inputs is performed at the floating gate, which in turn controls the ON/OFF state of the MOS transistor. Depending whether the weighted sum is above or under the intrinsic threshold voltage of the transistor, it can be fired on [1, 2]. Taking advantage of this feature, this device can be used to configure a circuit that can perform all the Boolean functions in a different fashion as that followed with conventional CMOS logic gates since using only one basic configuration any desired logic function can be obtained, just changing external voltages applied to programmable inverters. This approximation is called Soft Hardware Logic. A great difference in the construction of logic functions is found if the number of devices used in SHL circuits compared with conventional gates. For example, using the SHL technique, a full adder can be made using only 8 CMOS transistors while a design with conventional CMOS gates will use 50 transistors [2]. However, a drawback with SHL implementations is the large capacitance created by the weighted inputs, since their area may be large, affecting the speed of the logic.

II. *FLOATING-GATE POTENTIAL DIAGRAM.*

Since any voltage present on the floating-gate of the neu-MOS will determine the output of configurations like CMOS inverters, it is helpful to anticipate the voltage present at the floating gate for every combination of digital inputs feeding the input gates of the neu-MOS; this task as well as the determination of the number of programmable inverters, can be made with the Floating-gate Potential Diagram. Based on this methodology, weighted inputs for the input control gates of the neu-MOS can be derived. Fig. 1 shows the basic configuration used in this work for the analysis and design of a four bits input ALU and the corresponding FPD representing a XOR logic function, but this circuit can behave either as AND, NAND, OR, NOR, XOR and XNOR logic gates if voltages V_A,..,V_F are properly selected as needed for each gate, as is shown in [3]. The basic circuit is configured with a pre-charge input stage consisting in a CMOS inverter with a common floating gate. V_P is the multi-valued output from the pre-charge stage that depends on the digital inputs (4 bits). In Fig. 1, the four bits are represented only by one input in order to convert it to a multi-valued signal for simulation purposes. V_0 and V_F are used to adjust the output needed from the pre-charge stage. The intermediate stage consists on programmable inverters, V_A,..,V_E, needed for programming the transition across the threshold shown in Fig. 2. Finally, the last stage is the ν-MOS, where weighted inputs feed the floating gate to fire the CMOS inverter according to digital inputs. A detailed description of the basic circuit can be found in [3].

Fig. 2 shows the corresponding FPD for an XOR gate function completely referred to the ν-MOS stage. First, from Figure 2 it should be noticed that the *x-axis* is divided into 16 subdivisions since a 4 bits input is considered for the case shown. This is useful as a reference for the determination of the threshold voltage of the programmable inverters regarding the gate that is being designed and, in general, this is derived from the number of input bits, as follows:

IEEE Catalog Number: CFP12827-CDR
ISBN: 978-1-4673-2168-6
978-1-4673-2169-3/12/$31.00 ©2012 IEEE

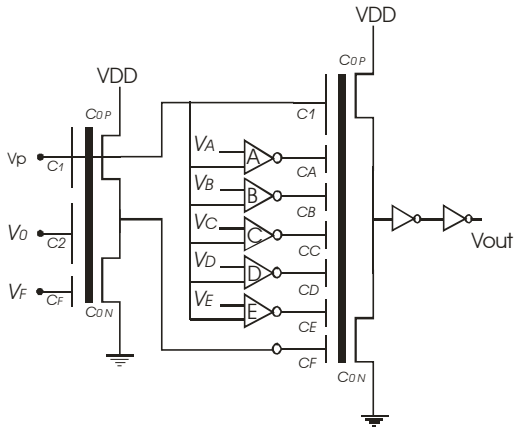


Fig. 1. Basic configuration of a 4-b νMOS SHL circuit.

$$\#subdiv_{.(x\text{ - axis})} = 2^N \tag{1}$$

where N is the number of bits considered. Also, the number of subdivisions in the *y-axis*, should be:

$$\#subdiv_{.(y\text{ - axis})} = 2*2^N \tag{2}$$

Furthermore, the magnitude of the coupling capacitances can be determined in terms of the floating-gate device gain γ, which corresponds to the ratio of the sum of the coupling capacitances to the total capacitance, equation (3). In this case, the ordinate, ϕ_F, is divided into 32 divisions with γV_{DD} as its maximum. From Fig. 2, the *y-axis* can be used either to read voltage (Floating-gate Potential, right axis) or capacitance (left axis), having in this case, a maximum magnitude of γV_{DD} or γC_{TOT}, respectively.

$$\gamma = \frac{C_1 + C_A + C_B + C_C + C_D + C_E + C_F}{C_{TOT}} \tag{3}$$

$$C_{TOT} = C_0 + C_1 + \ldots + C_n \tag{4}$$

Note that C_1 and C_F have the same value in the pre-charge and the ν-MOS stages.

$$C_0 = C_{ON} + C_{OP} \tag{5}$$

$$C_1 = C_{X_1} + C_{X_2} + C_{X_3} + C_{X_4} \tag{6}$$

$$\phi_F = \left(\frac{1}{C_{TOT}}\right)\left(V_P C_1 + V_A C_A + \cdots + V_F C_F\right) \tag{7}$$

where C_{0N} and C_{0P} are the channel capacitances of the NMOS and PMOS transistors of the ν-MOS inverter, respectively. C_1 is shared with the first and last stages and is the sum of the coupling capacitances included for the 4 bits at the input.

The bold solid line in Fig. 2 represents the voltage at the floating gate(ϕ_F) of the output stage (ν-MOS) as V_P goes from 0V to V_{DD} (5V for the case illustrated). The base line corresponds to ϕ_F of the ν-MOS when inputs at C_1, C_A, C_B, C_C, C_D, C_E and C_F are zero. The threshold line corresponds to $\gamma V_{DD}/2$, such that:

$$\text{if } \phi_F > \gamma V_{DD}/2 \quad \text{Vout=high}$$

$$\phi_F < \gamma V_{DD}/2 \quad \text{Vout=low}$$

Thus, it should be noticed that the FPD shown in Fig. 2 follows the truth table for a 4 bits XOR logic gate. Besides, extrapolating the slope of each transition seen in the FPD, the magnitude of the coupling capacitances can be read from the left *y-axis*. In this case, the ratios for the corresponding coupling capacitances are:

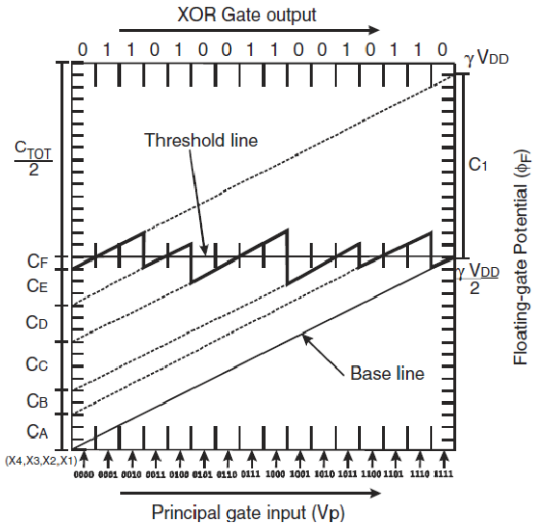


Fig. 2. Theoretical Floating-gate Potential Diagram (FPD) for the main νMOS inverter in Fig. 1. The case for the XOR gate is illustrated.

$$C_1 = \frac{15}{32}\gamma C_{TOT}$$

$$C_A = \frac{3}{32}\gamma C_{TOT} \qquad C_B = \frac{2}{32}\gamma C_{TOT} \qquad C_C = \frac{4}{32}\gamma C_{TOT}$$

$$C_D = \frac{3}{32}\gamma C_{TOT} \qquad C_E = \frac{3}{32}\gamma C_{TOT} \qquad C_F = \frac{1}{32}\gamma C_{TOT}$$

Finally, a programmable CMOS inverter like those used in the intermediate stage is shown in Figure 3. Each one of these inverters is biased with voltages V_A through V_F together with V_P in order to present a transition according to the logic gate desired.

IEEE Catalog Number: CFP12827-CDR
ISBN: 978-1-4673-2168-6
978-1-4673-2169-3/12/$31.00 ©2012 IEEE

III. BINARY CIRCUIT DESIGN.

Using the methodology described in detail in [3], individual SHL gates were designed. Then a configuration is proposed to construct a basic ALU. The method followed for designing and implementing an n-bit logic gate using a neu-MOS transistor is presented. Basically, a 4-bit unit was designed to operate like XOR logic gate, as is needed for an adder circuit, which is the core of the pretended ALU. The full adder accepts three 4-bits inputs: summands A and B and the carry input, Cin. The outputs from the full adder are F (*sum*) and Cn (*carry out*). The output signals are ruled by the following Boolean equations:

$$F\ (sum) = A \oplus B \oplus Cin. \quad (8)$$

$$Cn\ (carry\ out) = A \bullet B + (A \oplus B) \bullet Cin \quad (9)$$

Actually, the proposed unit is capable to perform 2 Arithmetic and 2 Logic functions, from this basic design, but the operations capability can be extended as well, with a more complex design. The signal used to select and control the desired operations in this ALU as it is proposed, is a four bit input signal S.

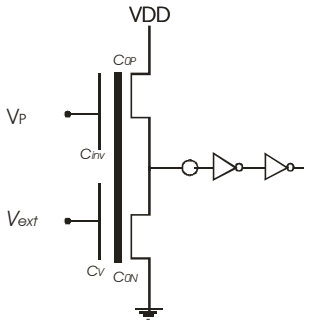


Fig. 3. Configuration of one programmable inverter, where *Vp* corresponds to the 4-b input and *Vext* is the external voltage input *VA* through *VF*, corresponding to each programmable inverter used.

However, a large variety of logic and arithmetic operations can be performed with the presented methodology, but for simplicity and space limitations, the selected operations to demonstrate the feasibility of the ALU designed with this methodology will be:

Logic: A and B, A xnor B

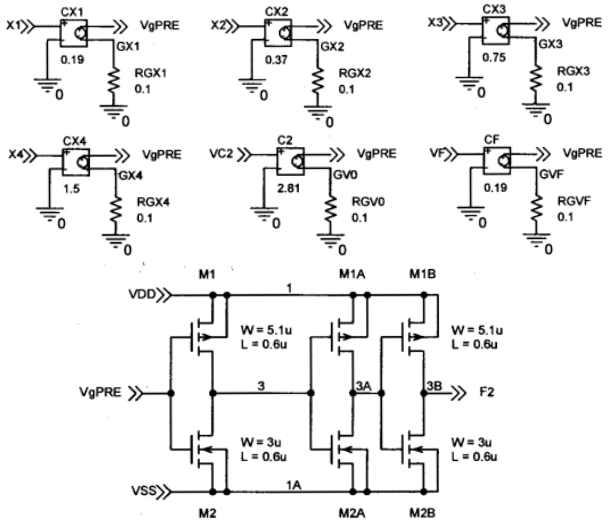
Arithmetic: A+B, A●B-1

Besides, in order to have a reference from which a comparison can be made, output for these operations were obtained first with a synthesized ALU designed with a FPGA evaluation kit (Spartan 3E, from Xilinx) and also with the Motorola's MC14581B ALU chip, with 4 bits input too, while the design developed with SHL was simulated with ORCAD. Fig. 4 shows the schematic diagram of the universal circuit employed to configure each of the gates needed to perform the selected arithmetic and logic functions. As can be seen, the circuit is based on voltage controlled voltage sources to represent the voltage at the floating gate of the ν-MOS and the programmable inverters. Depending on the logic gate to be configured, the voltages V_A, V_B, V_C, V_D, V_E and V_F must be modified using the values shown in Table I.

TABLE I.
EXTERNAL VOLTAGES APPLIED TO THE PROGRAMMABLE INVERTERS.

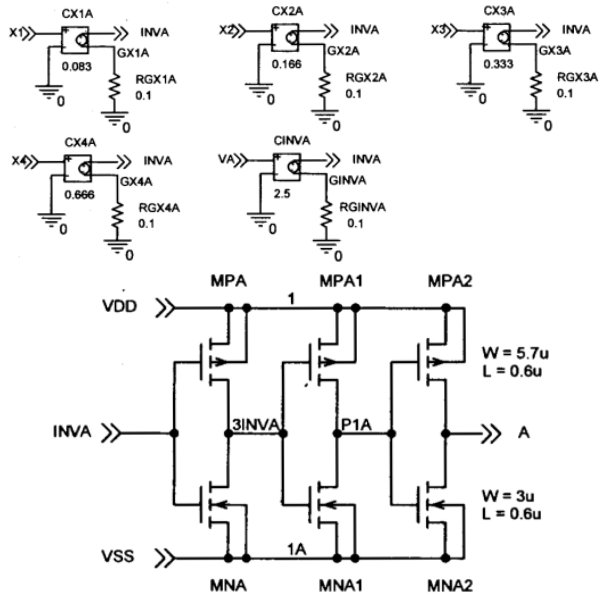
	External voltages applied to the programmable inverters depending on the desired logic gate (V).						
Logic function	V_A	V_B	V_C	V_D	V_E	V_F	V_{C2}
XNOR	4.79	4.33	3.86	3.23	2.92	0	0
NOR	4.81	4.81	4.81	4.81	4.81	4.81	4.5
AND	5	5	5	5	5	0.25	0
NAND	2.6	2.6	2.6	2.6	2.6	2.6	0.24
OR	2.41	2.41	2.41	2.41	2.41	2.45	5
XOR	2.61	3.08	3.55	4.17	4.48	4.97	5

Notice that the pre-charge input MOS inverter has 6 sources representing the digital inputs C_{X1}, C_{X2}, C_{X3}, C_{X4}, and the adjusting inputs C_2 and C_F. The programmable inverter used 5 sources representing C_{X1}, C_{X2}, C_{X3}, C_{X4} and V_{ext}. Finally, the ν-MOS uses 10 sources for C_{X1}, C_{X2}, C_{X3}, C_{X4}, and C_A, C_B, C_C, C_D, C_E and C_F, from the programmable inverters.

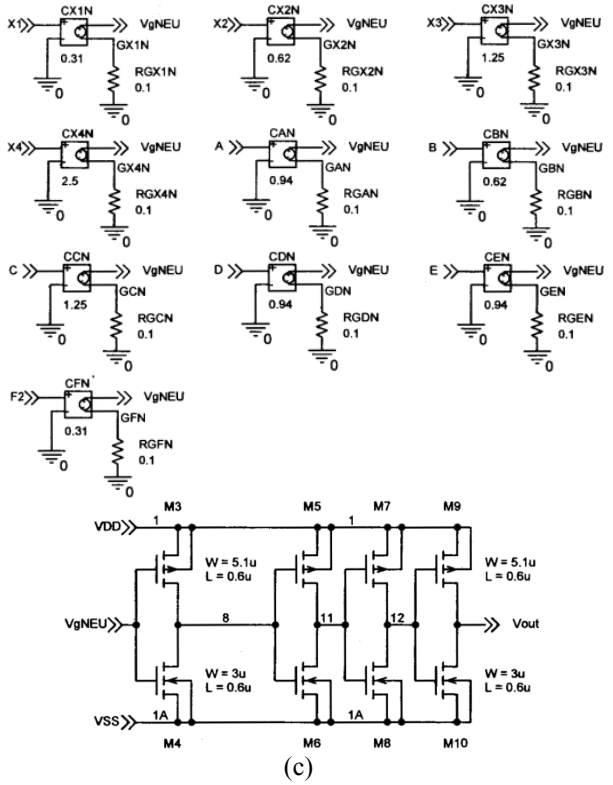


(a)

IEEE Catalog Number: CFP12827-CDR
ISBN: 978-1-4673-2168-6
978-1-4673-2169-3/12/$31.00 ©2012 IEEE



(b)



(c)

Fig. 4. Schematic diagram of the universal circuit used for logic gates configured with SHL: a) pre-charge input; b) programmable inverter; c) ν-MOS inverter.

IV. Results

Due to the large combinations that can be input to the ALU (2^4 x 2^4 = 256), the results presented for measurements and simulations will illustrate only a few output examples of the arithmetic and logic operations to demonstrate the proper performance of the SHL circuit compared with the commercial chip and the FPGA implementation. Fig. 5 shows the block diagram of the SHL-ALU.

Tables II, III and IV describe the operations selected as a function of the selection key, S, referred to Fig. 5.

TABLE II
OPERATION SELECTION FOR THE BLOCK F1.

S0	S1	F1
0	0	**A•B**
0	1	**A**
1	0	**B**
1	1	**A XNOR B**

TABLE III
OPERATION SELECTION FOR THE BLOCK F2.

S3	S2	F2
0	0	**0**
0	1	**A**
1	0	**B**
1	1	**1**

TABLE IV
OPERATION SELECTION FOR THE BLOCK fcarry.

Y	X	Cin	X+Y	fcarry
0	0	0	0	**0**
0	0	1	1	**0**
0	1	0	1	**0**
0	1	1	0	**1**
1	0	0	1	**0**
1	0	1	0	**1**
1	1	0	0	**1**
1	1	1	1	**1**

TABLE V
KEY SELECTION FOR LOGIC AND ARITH. OPERATIONS.

S3	S2	S1	S0	Output Function
0	0	0	0	**A and B**
0	0	1	1	**A xnor B**
1	0	0	1	**A + B**
1	1	0	0	**A•B - 1**

A. Arithmetic operations

1) A+B: Fig. 6 shows the plot for this operation with the output measured to the chip, the FPGA implementation and the SHL ALU. The experimental frequency of excitation used was 4.167MHz. From the figure it can be seen that the results are the same in the three cases. The results presented

IEEE Catalog Number: CFP12827-CDR
ISBN: 978-1-4673-2168-6
978-1-4673-2169-3/12/$31.00 ©2012 IEEE

correspond to values for A=[8,9,10,11] while B=[0,…,15] for each value of A.

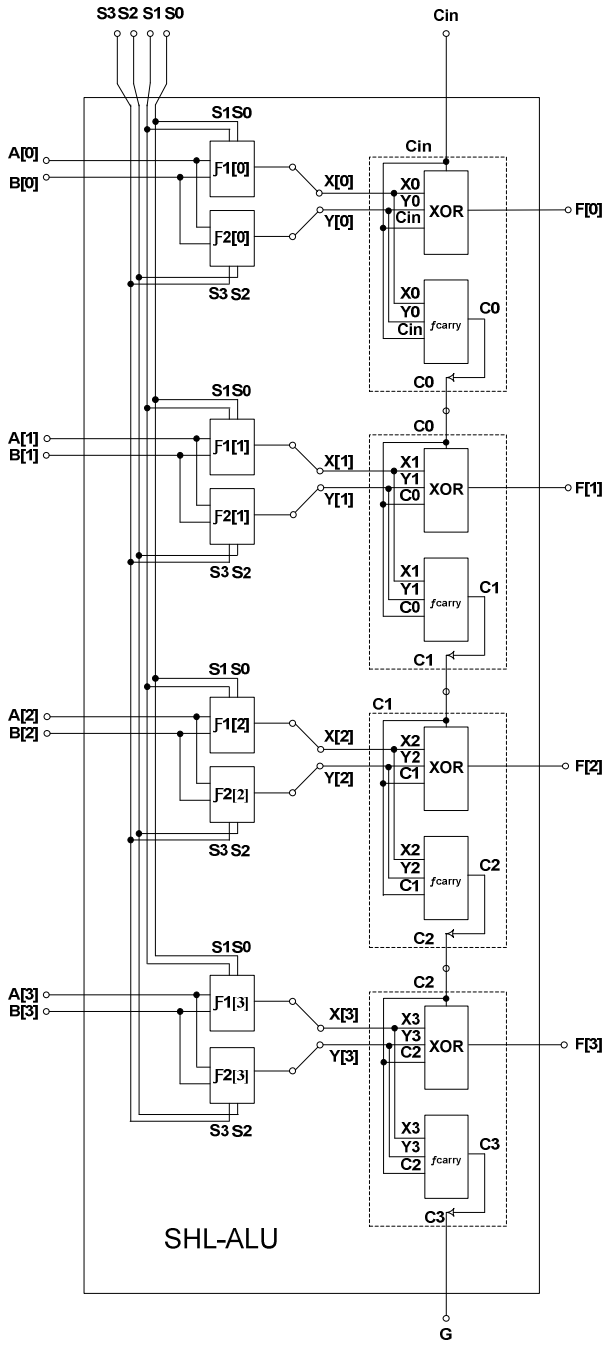


Fig. 5. Block diagram of the proposed ALU designed with SHL.

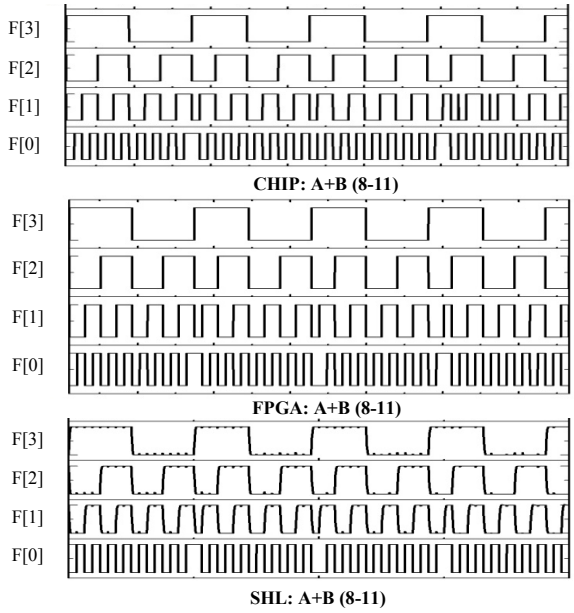


Fig. 6. Output comparison for the three ALU configurations with the arithmetic operation A+B.

2) AB-1: Figure 7 shows the comparison for this arithmetic operation using the same excitation conditions as before

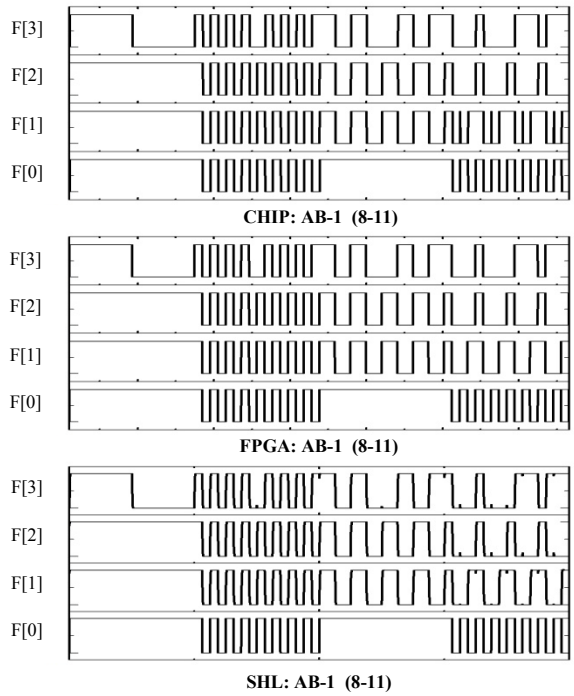


Fig. 7. Output comparison for the three ALU configurations with the arithmetic operation AB-1.

IEEE Catalog Number: CFP12827-CDR
ISBN: 978-1-4673-2168-6
978-1-4673-2169-3/12/$31.00 ©2012 IEEE

3) AB: Fig. 8 corresponds to this logic operation with the same excitation and frequency input as before.

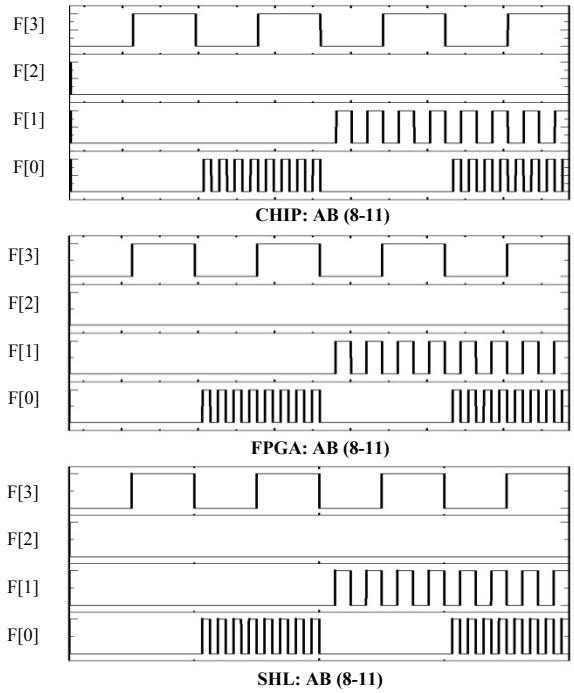


Fig. 8. Output comparison for the three ALU configurations with the logic operation AB.

4) A xnor B: Finally, Figure 9 shows the last logic operation compared for the three configurations.

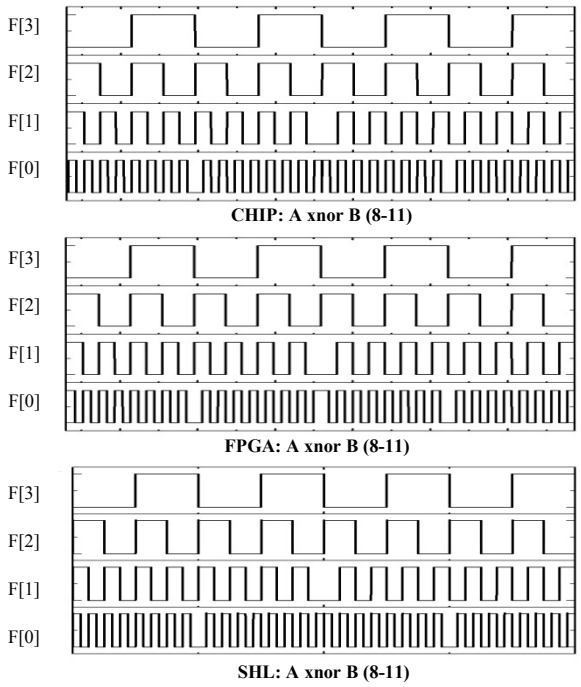


Fig. 9. Output comparison for the three ALU configurations with the logic operation A xnor B.

From these last figures, it can be concluded that the methodology proposed is reliable to be used as a digital alternative for circuit design, although a deep study should still be made since there are also issues like frequency limits, power dissipation and control signals for operation selection that must be established.

The Stimulus applied to the SHL Circuit is shown in Fig. 10.

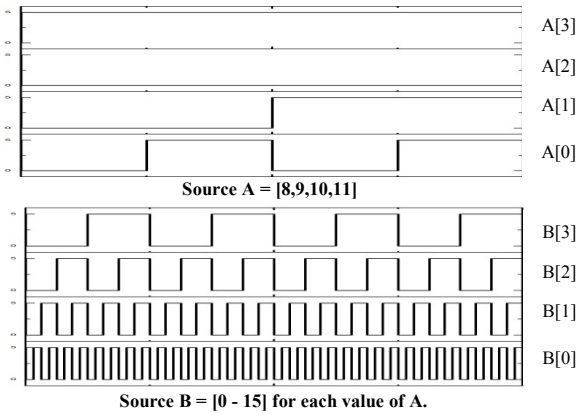


Fig. 10. Stimulus applied to the SHL Circuit, where input A takes the values [8,9,10,11], whereas B takes values from 0 to 15 for each value of A.

V. Conclusions

The applications of the ν-MOS transistor can be extended to the digital dominium through the Soft-Hardware-Logic methodology, based in the Floating-gate Potential Diagram. With this alternative, reconfigurable basic cells like logic gates can be designed giving an interesting option for digital circuits. Furthermore, subsystems like adders can be configured and used for designing more complex blocks like an Arithmetic Logic Unit, for instance, although there is still work to do regarding frequency operation and area integration issues, among others.

References

[1] T. Shibata and T. Ohmi, "Neuron MOS Binary-Logic Integrated Circuits- Part I: Design Fundamentals and Soft-Hardware-Logic Circuit Implementation", *IEEE Trans. on Electron Devices*, Vol. 40, No. 3, pp .570-576, March 1993.

[2] T. Shibata and T. Ohmi, "Neuron MOs Binary-Logic Integrated Circuits- Part II: Simplifying Techniques of Circuits Configuration and Their Practical Applications", *IEEE Trans. on Electron Devices*, Vol. 40, No. 3, pp. 974-979, May 1993.

[3] M.A. Reyes-Barranca and A. Medina-Santiago "Methodology for the design of a 4-bit Soft-Hardware-Logic circuit based on neuron MOS transistors", *International Journal of Electronics*, 95:6, 2008, 517-530.

[4] J.Ramírez-Angulo, G. González-Altamirano and S.C. Choi, "Modelling Multiple-input Floating-gate Transistor for analogue Signal Processing", *IEEE International Symposium on Circuits and Systems*, June, 9-12, 1997, Hong Ko.

IEEE Catalog Number: CFP12827-CDR
ISBN: 978-1-4673-2168-6
978-1-4673-2169-3/12/$31.00 ©2012 IEEE